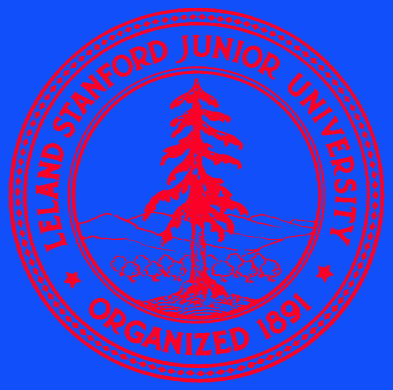
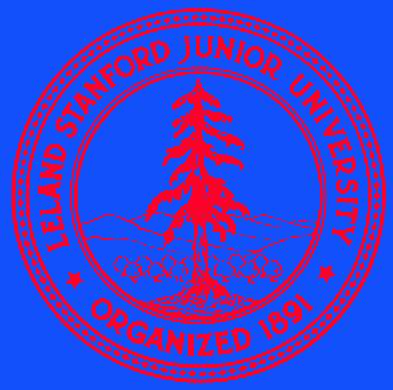
MICROMACHINING PROCESSES

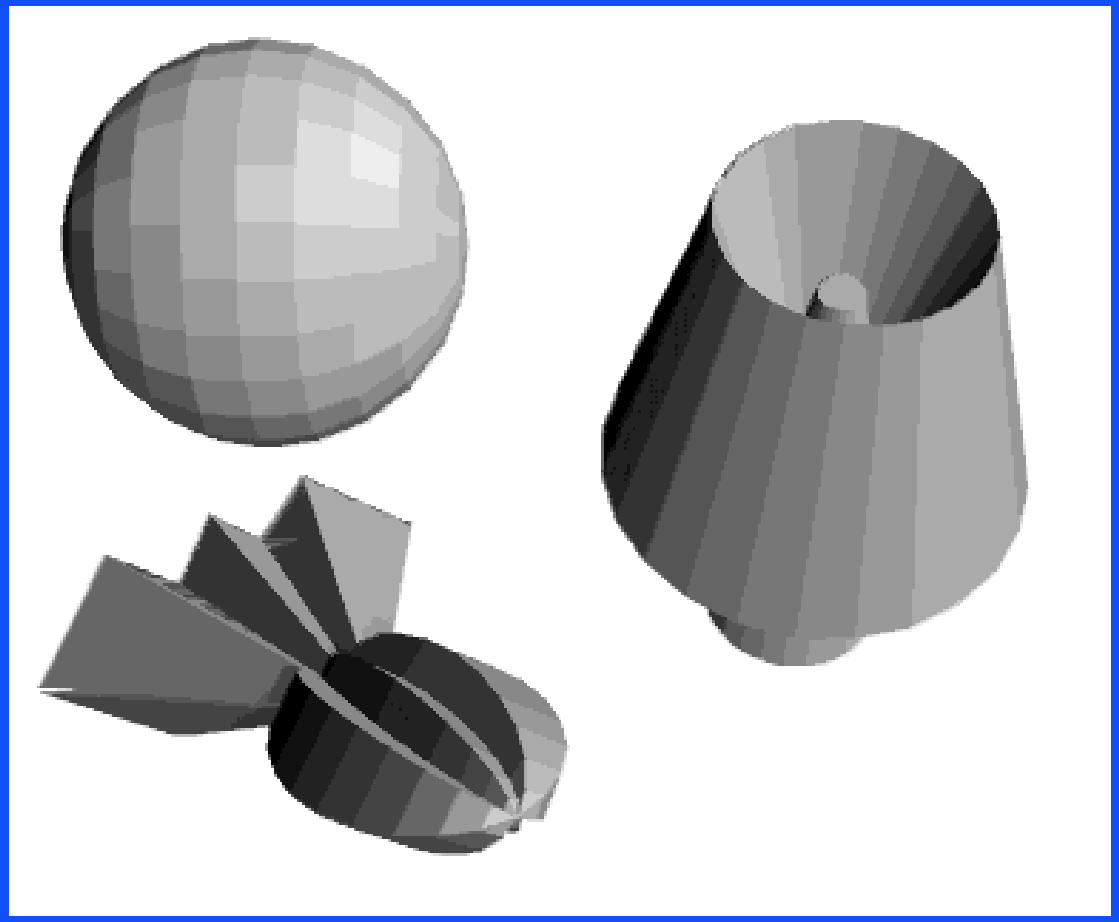
EE312, Prof. Greg Kovacs



Stanford University



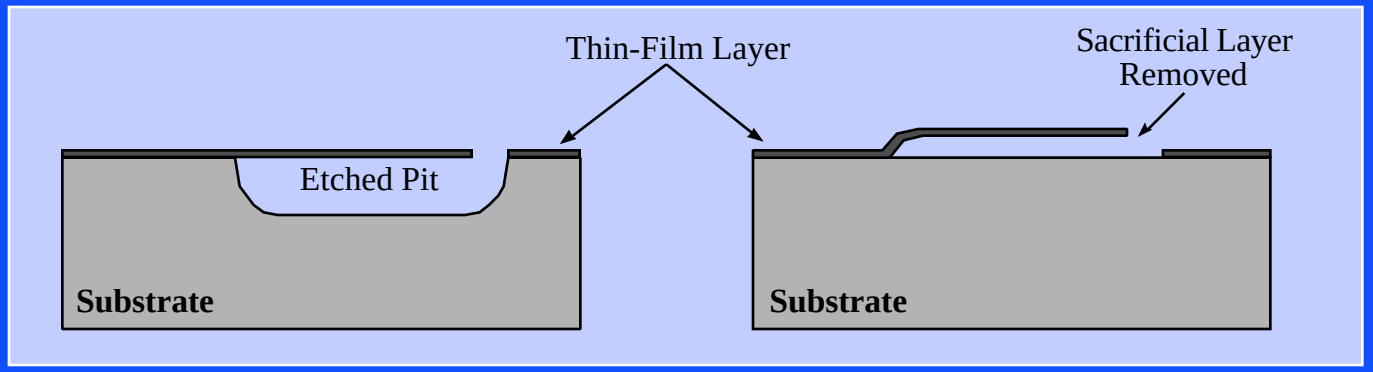
SOME SHAPES ARE DIFFICULT TO FABRICATE LITHOGRAPHICALLY

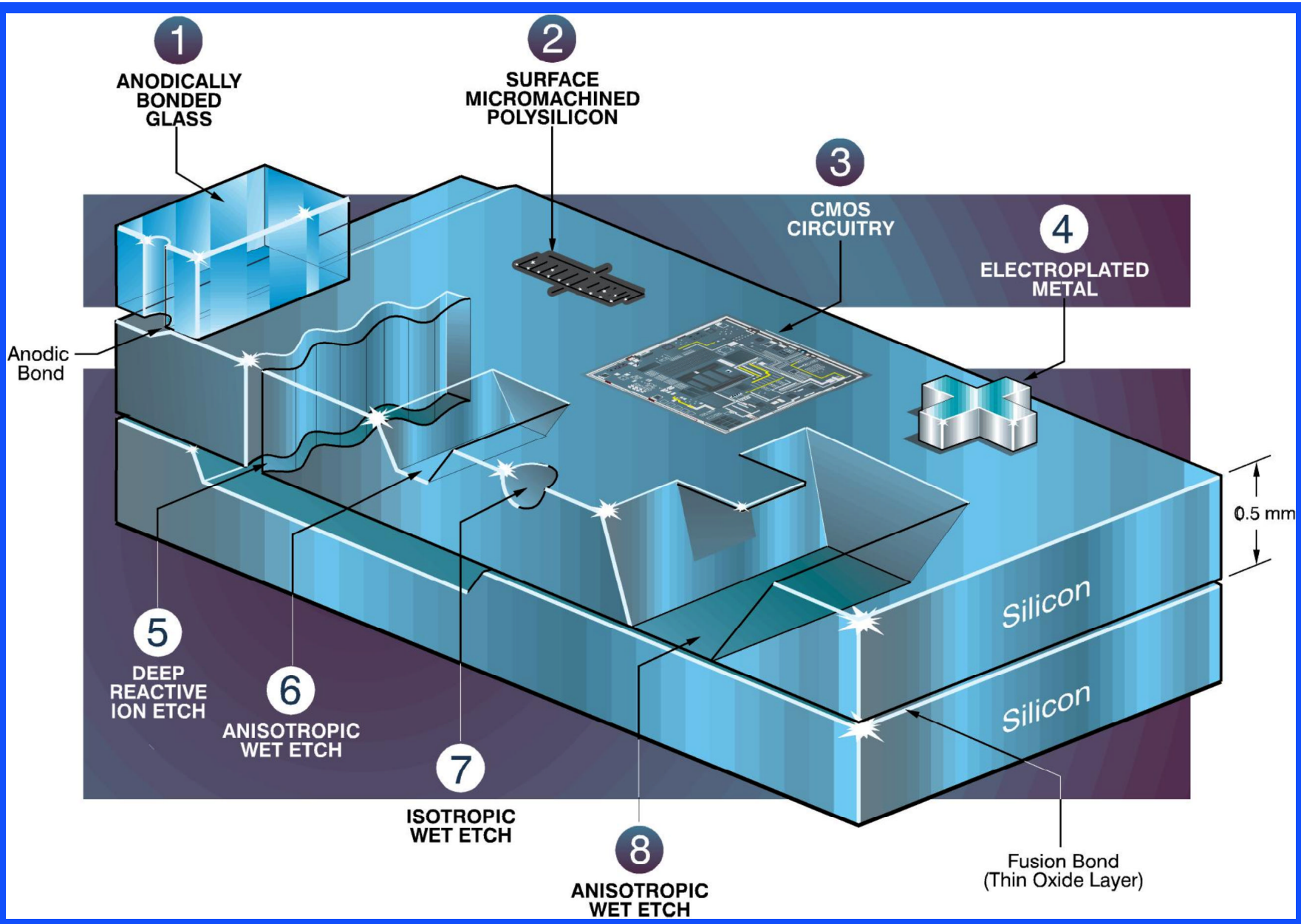


A key goal is to learn what can and what cannot be micromachined.

ADDITIVE AND SUBTRACTIVE PROCESSES

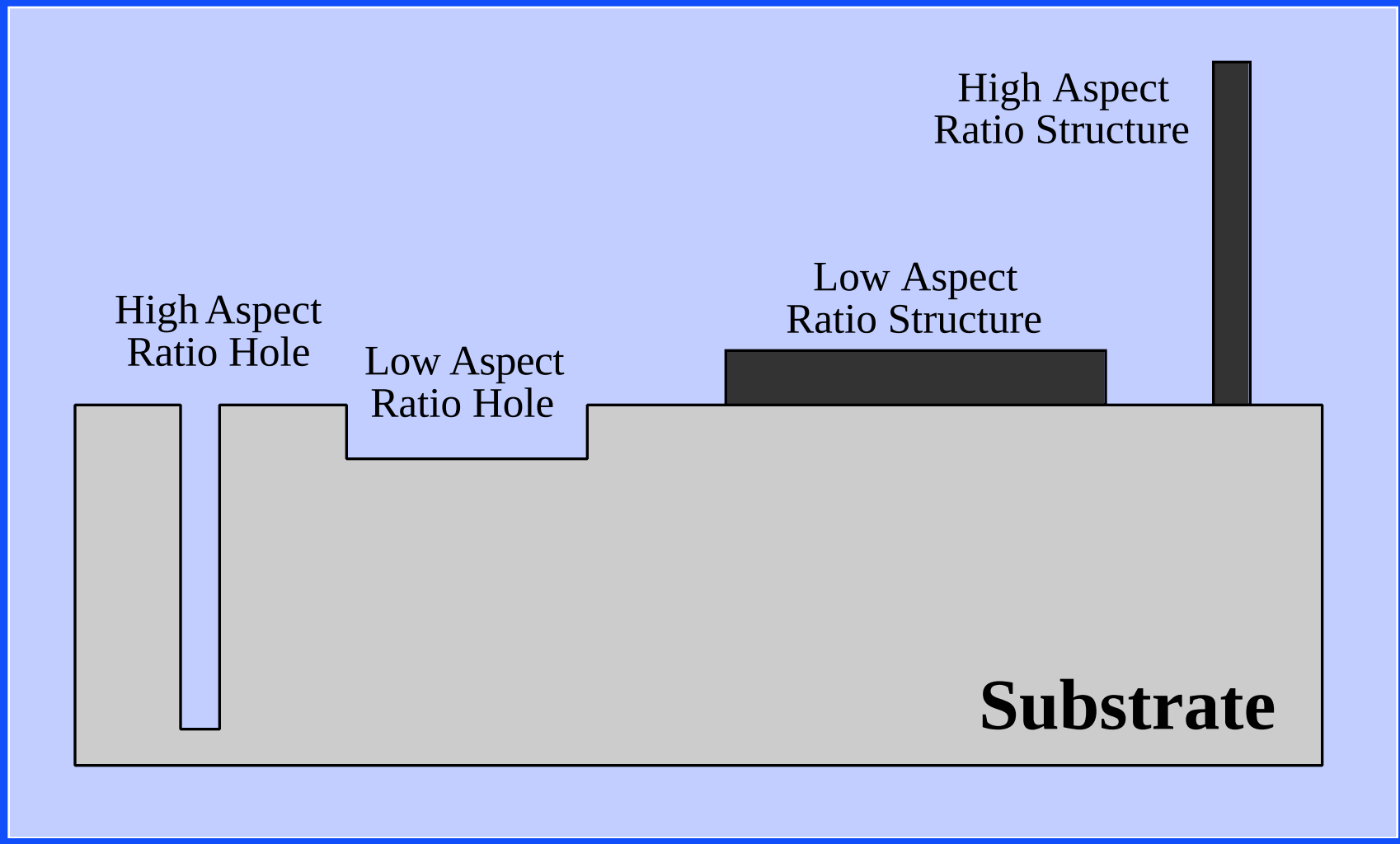
- **Micromachining processes generally fall into the two categories of *additive* and *subtractive*.**
- **Subtractive processing involves removal of appreciable regions of the substrate (usually silicon, but possibly glass, organics, metals, etc.).**
- **Additive processing involves adding material(s) above the substrate (processes such as thin-film deposition, electroplating, etc.).**
- **In some cases, "sacrificial" layers are removed after additive steps to form voids or free isolated regions.**





Concept: G. Kovacs Illustration: R. Thomas

ASPECT RATIO



SUBSTRATES FOR MICROMACHINING

- Silicon and other elemental semiconductors.
- Silicon-on-insulators.
- GaAs and other compound semiconductors.
- Metals (bulk and foils).
- Glasses.
- Quartz.
- Ceramics.
- Plastics, polymers and other organics.

ADDITIVE MATERIALS FOR MICROMACHINING

- Silicon (epitaxial, polysilicon, amorphous).
- Silicon compounds (nitrides, oxides, carbides, etc.).
- Metals and metal compounds.
- Ceramics
- Organics (including biomolecules).

GENERAL PROPERTIES @ 300 K	Si	Ge	GaAs
Atomic Weight	28.09	72.60	144.63
Density (g/cm^3)	2.328	5.3267	5.32
Atomic Density ($atoms/cm^3$)	5.0×10^{22}	4.42×10^{22}	4.42×10^{22}
Lattice Constant Å	5.43095	5.64613	5.6533
THERMAL PROPERTIES			
Melting Point (°C)	1,415	937	1,238
Specific Heat (J/g•K)	0.7	0.31	0.35
Linear Coeff. of Thermal Expansion ($\alpha = \Delta L/(L\Delta T)$, in K^{-1})	2.6×10^{-6}	5.8×10^{-6}	6.86×10^{-6}
Thermal Conductivity (at 300 K) (W/cm•K)	1.5	0.6	0.46
Thermal Diffusivity (cm^2/s)	0.9	0.36	0.24
ELECTRICAL PROPERTIES			
Energy Gap (eV) at 300 K	1.12	0.66	1.424
Intrinsic Carrier Concentration (cm^{-3})	1.45×10^{10}	2.4×10^{13}	1.79×10^{6}
Intrinsic Resistivity (Ω•cm)	2.3×10^{5}	47	10^{8}
Dielectric Constant (DC only)	11.9	16.0	13.1
* Breakdown Field (V/cm)	$\approx 3 \times 10^{5}$	$\approx 10^{5}$	$\approx 4 \times 10^{5}$
* Minority Carrier Lifetime (s)	2.5×10^{-3}	10^{-3}	$\approx 10^{-8}$
* Electron Mobility ($cm^2/V•s$)	1,500	3,900	8,500
* Hole Mobility ($cm^2/V•s$)	450	1,900	400

COMMON SEMICONDUCTORS FOR MICROMACHINING

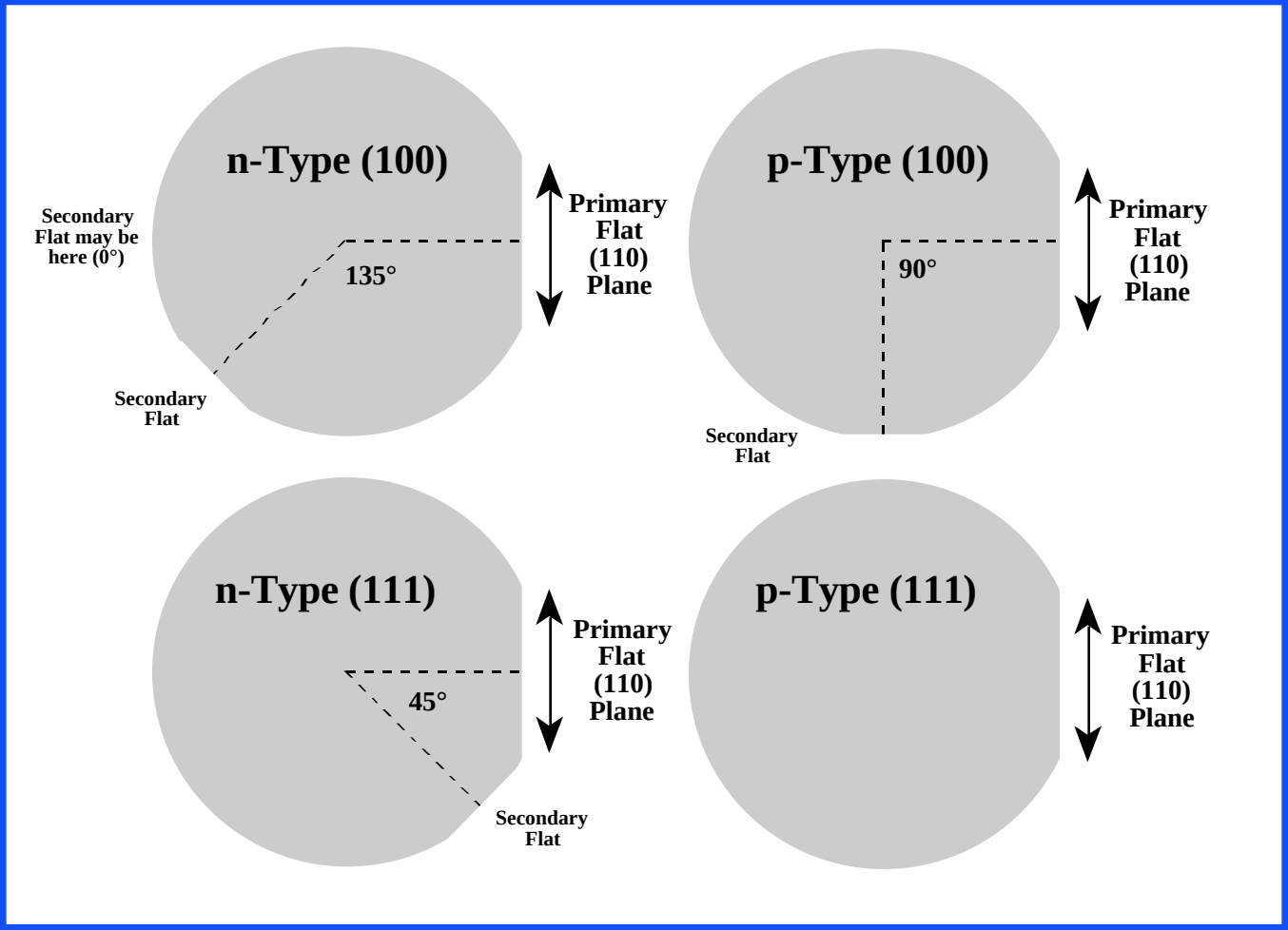
WHY USE SILICON?

- **Readily available in high-quality form.**
- **Properties very well known.**
- **Can take advantage of prior process work.**
- **Have option of integrating active circuits.**

Material	Yield Strength (10^9 N/m^2)	Knoop Hardness (kg/mm^2)	Young's Modulus (GPa)	Density (g/cm^3)	Thermal Conductivity (W/cm•K)	Thermal Expansion Coefficient (10^6/K)
*Diamond	53	7,000	1,035	3.5	20	1
*SiC	21	2,480	700	3.2	3.5	3.3
*TiC	20	2,470	497	4.9	3.3	6.4
*Al_2O_3	15.4	2,100	530	4	0.5	5.4
*Si_3N_4	14	3,486	385	3.1	0.19	0.8
*Iron	12.6	400	196	7.8	0.803	12
SiO_2 (fibers)	8.4	820	73	2.5	0.014	0.55
*Si	7	850	190	2.3	1.57	2.33
Steel (max strength)	4.2	1,500	210	7.9	0.97	12
W	4	485	410	19.3	1.78	4.5
Stainless Steel	2.1	660	200	7.9	0.329	17.3
Mo	2.1	275	343	10.3	1.38	5
Al	0.17	130	70	2.7	2.36	25

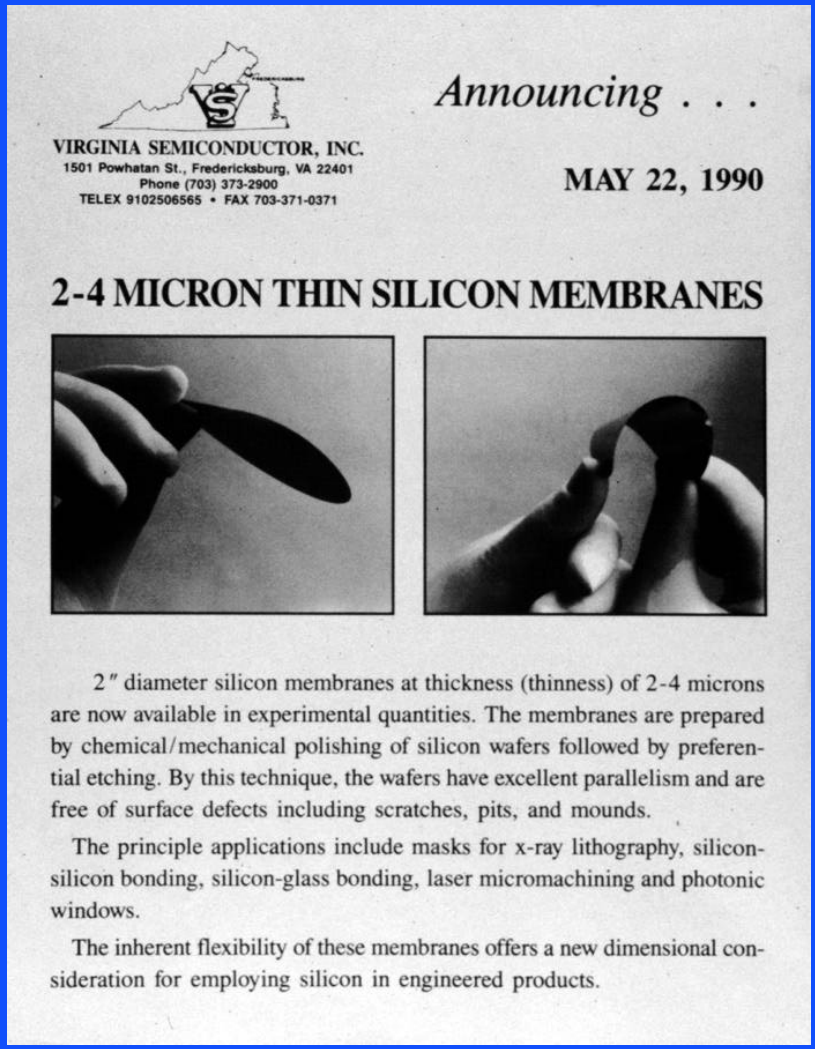
*** = single crystal data**

SILICON CRYSTAL ORIENTATIONS



A VARIETY OF SILICON SUBSTRATES ARE AVAILABLE

- There are several suppliers who have many crystal orientations, thicknesses, and grades of wafers.
- Many sizes are available, although 4” and smaller wafers are becoming rarer.
- Epitaxial layers are also available.
- Double-side-polished wafers can be obtained ready or the polishing can be done commercially.
- Some types of wafers are very expensive.



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Announcing . . .

MAY 22, 1990

2-4 MICRON THIN SILICON MEMBRANES

2″ diameter silicon membranes at thickness (thinness) of 2-4 microns are now available in experimental quantities. The membranes are prepared by chemical/mechanical polishing of silicon wafers followed by preferential etching. By this technique, the wafers have excellent parallelism and are free of surface defects including scratches, pits, and mounds.

The principle applications include masks for x-ray lithography, silicon-silicon bonding, silicon-glass bonding, laser micromachining and photonic windows.

The inherent flexibility of these membranes offers a new dimensional consideration for employing silicon in engineered products.

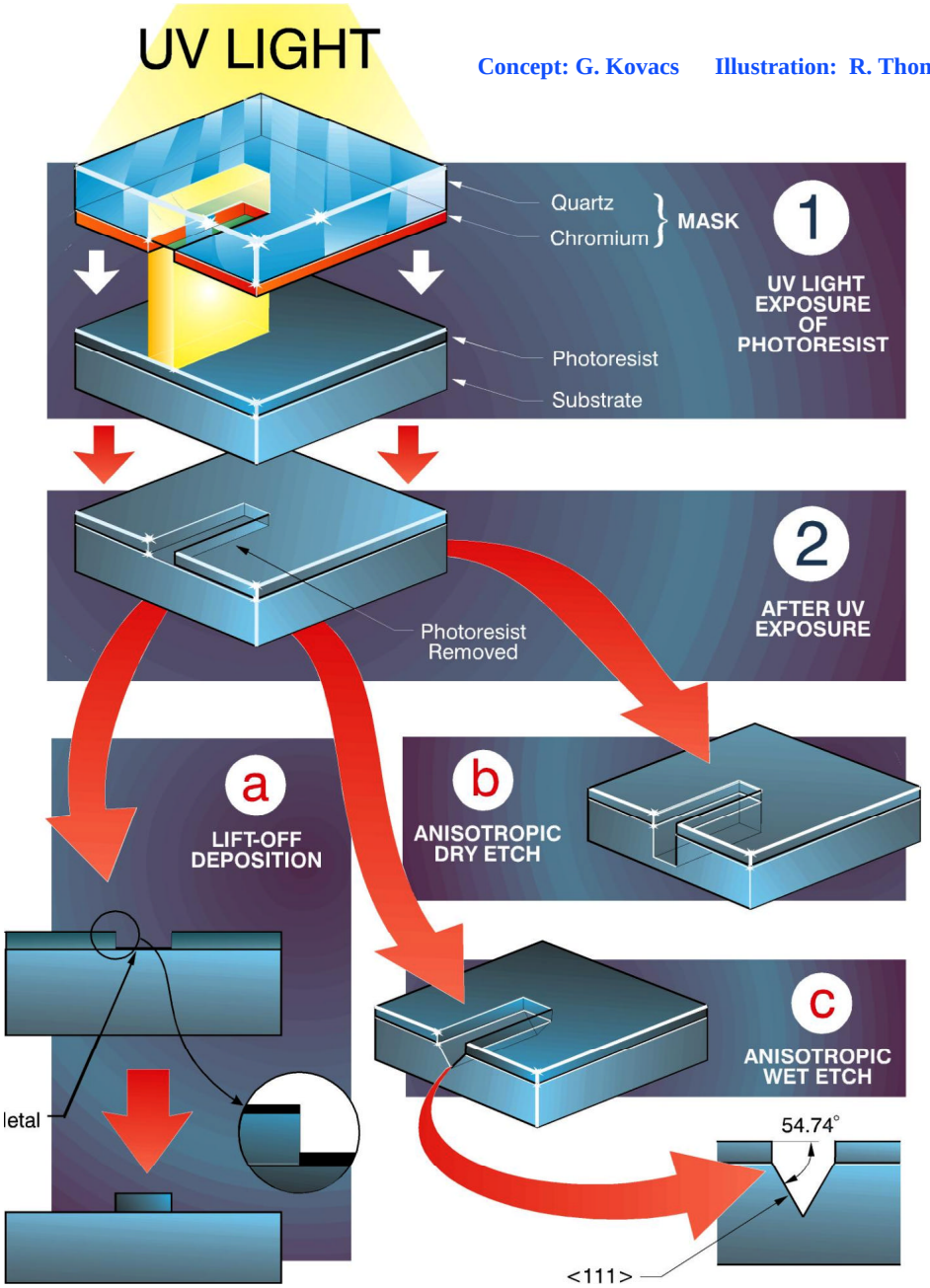
EXAMPLE PROCESSES

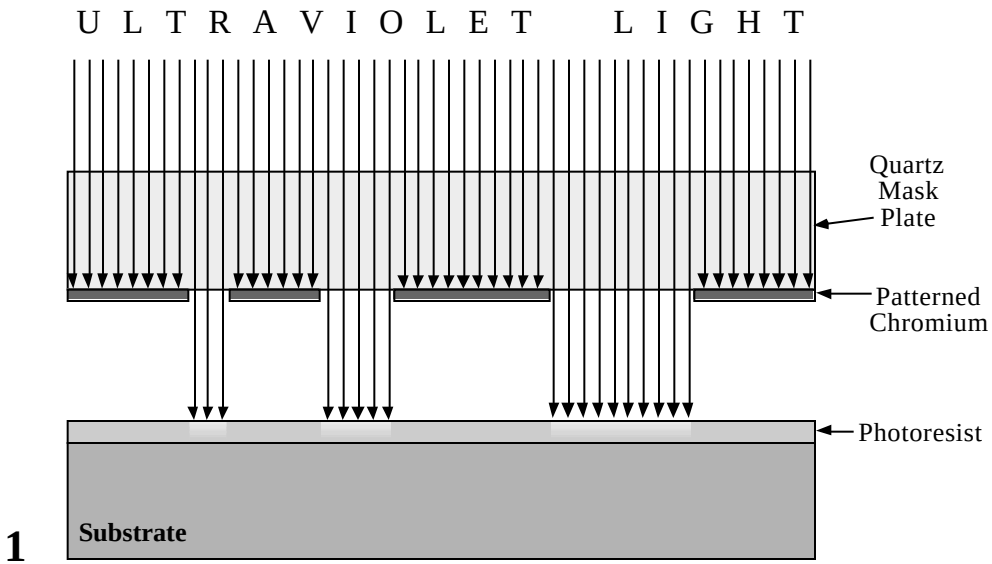
Process Type	Examples
Lithography	photolithography, screen printing, electron-beam lithogaphy, x-ray lithography
Thin-Film Deposition	chemical vapor deposition (CVD), plasma-enhanced chemical vapor deposition (PECVD), sputtering, evaporation, spin-on application, plasma spraying, etc.
Electroplating	blanket and template-delimited electroplating of metals
Directed Deposition	electroplating, stereolithography, laser-driven chemical vapor deposition, screen printing, transfer printing
Etching	plasma etching, reactive-ion enhanced (RIE) etching, deep reactive ion etching (DRIE), wet chemical etching, electrochemical etching, etc.
Directed Etching	laser-assisted chemical etching (LACE)
Machining	drilling, milling, electric discharge machining (EDM), diamond turning, sawing, etc.
Bonding	fusion bonding, anodic bonding, adhesives, etc.
Surface Modification	wet chemical modification, plasma modification
Annealing	thermal annealing, laser annealing

LITHOGRAPHY

- **Lithography is the basic technique used to define and transfer patterns in most micromachining and integrated circuit fabrication.**
- **In optical lithography UV light is directed through a mask to selectively expose a photosensitive organic material (photoresist).**
- **For positive-working resist, exposed resist is removed in developer.**
- **Exposed regions can be then be manipulated (etching, deposition, etc.) or the resist can be used as a sacrificial (temporary spacer) layer.**

LITHOGRAPHY





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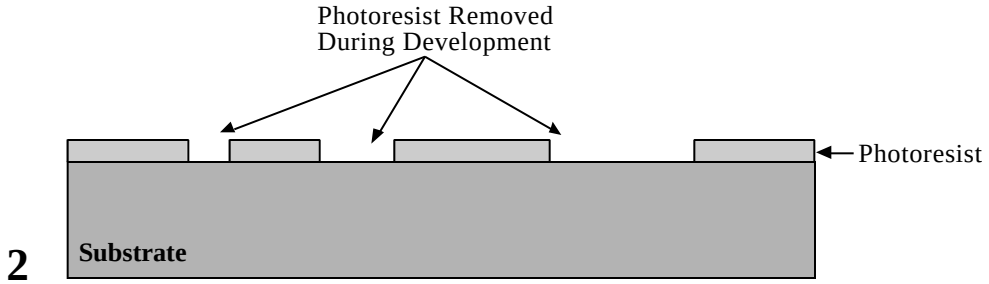

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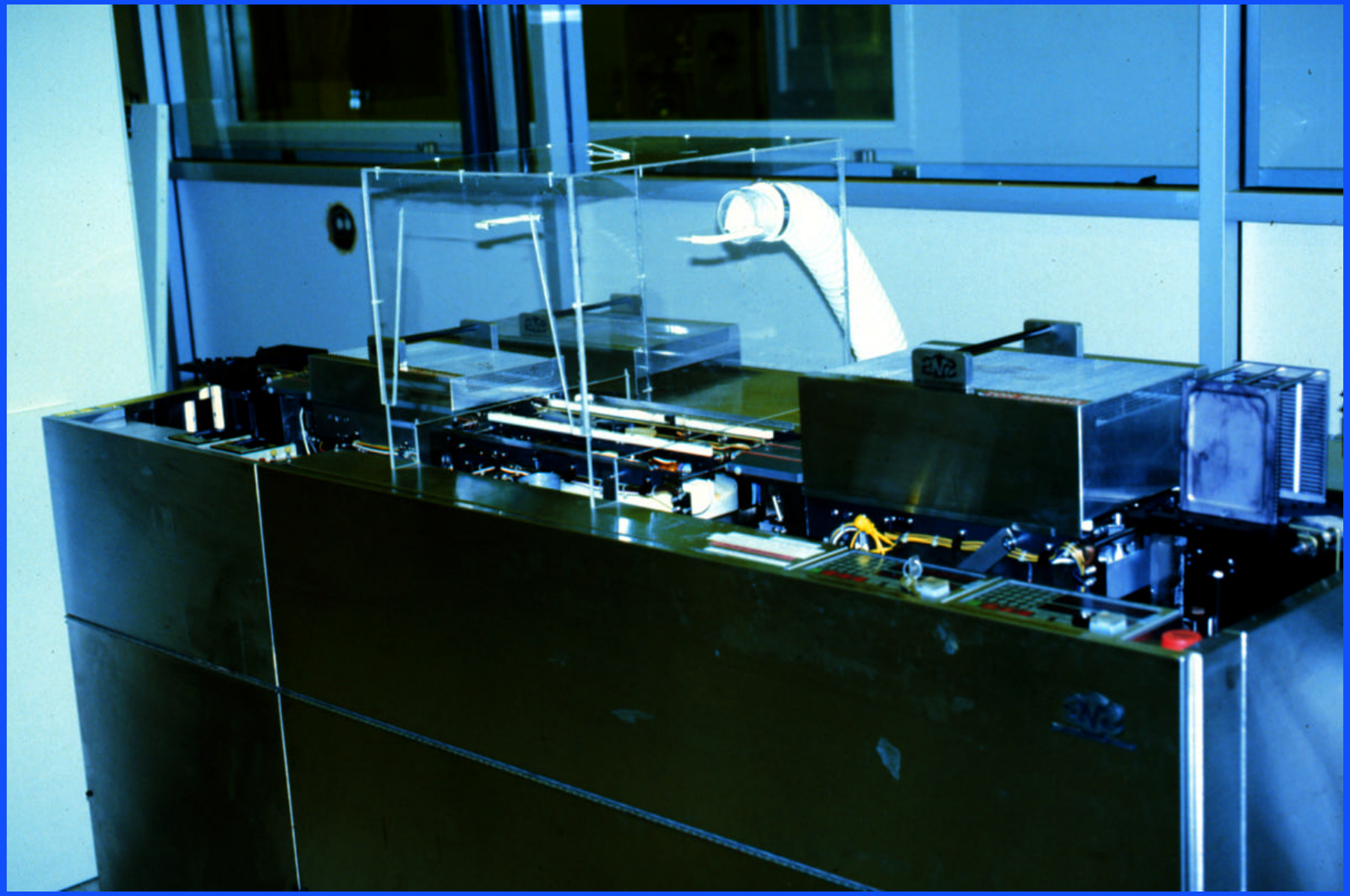
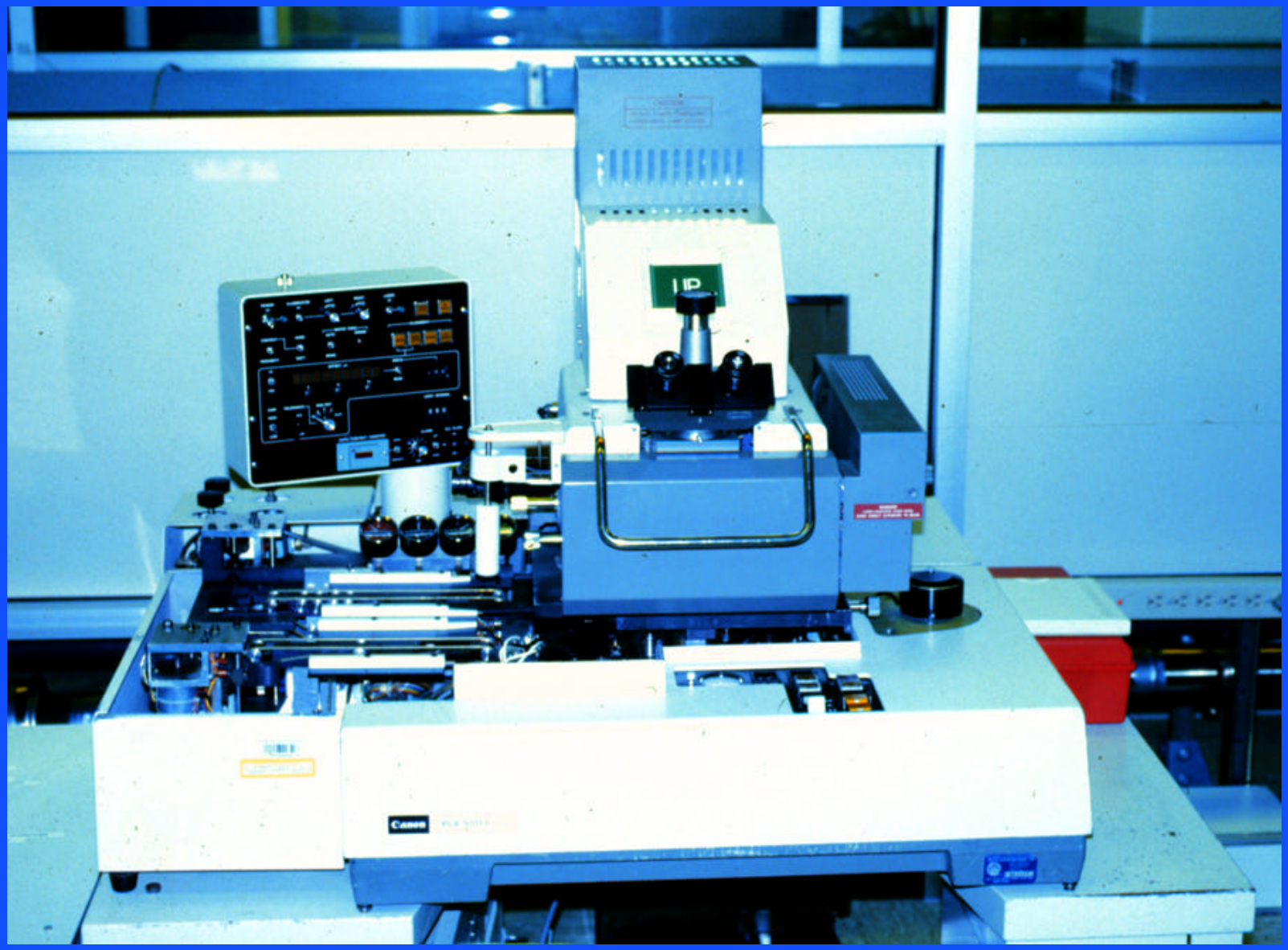
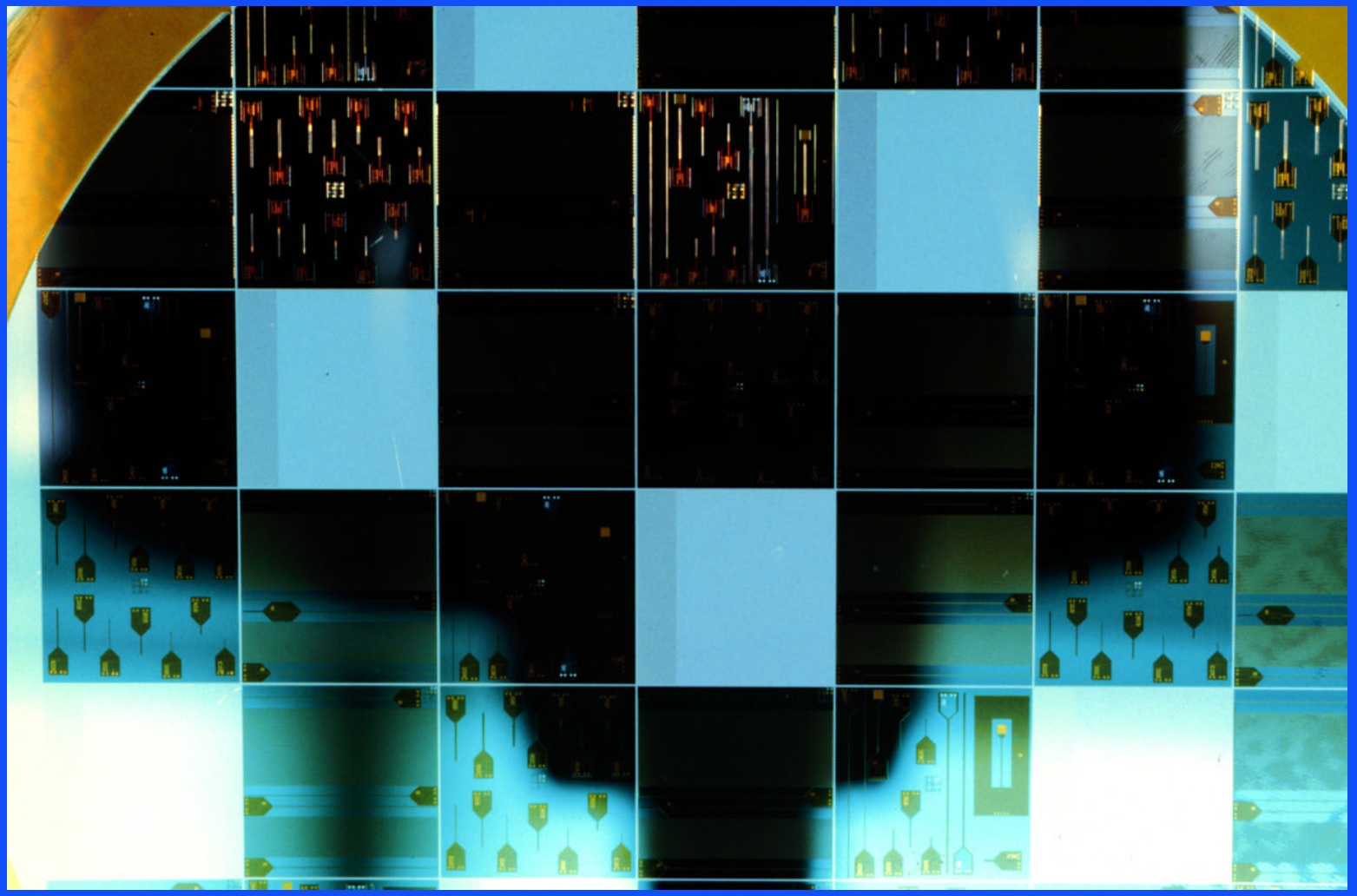
Courtesy Dr. Kurt Petersen, Lucas NovaSensor.





DISTINCT PATTERS OVER A WHOLE WAFER: DIFFICULT WITH A STEPPER



WET SILICON ETCHING

- **Most micromachining is presently done with silicon, and a large amount of that is etching with wet chemicals.**
- ***Isotropic* etchants (e.g. HNA) give rounded profiles.**
- ***Anisotropic* etchants (e.g. KOH, TMAH) slow down markedly on (111) crystal planes of silicon, yielding flat surfaces.**
- **Dopants such as high concentrations of boron can be used to stop the progress of etchants such as KOH.**
- **Electrochemical etch-stop techniques can also be used since at certain potentials, silicon forms an anodic oxide that stops etching.**

ETCHANT PROPERTIES

- Selectivity to masking layer(s) and their availability.
- Selectivity to metals (e.g. Al).
- Etch rate.
- Anisotropy (crystal plane selectivity).
- Surface roughness.
- Control of etch parameters.
- Safety of reactant(s) and product(s).
- Cost (including disposal and fixed costs).
- Capacity for etch-stops.
- Mode and ease of use (including throughput).
- Other parameters?

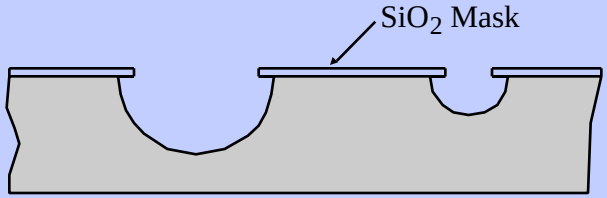
Comparison of Example Silicon Etchants

	HNA ($HF+HNO_3$ +Acetic Acid)	Alkali-OH	EDP (ethylene diamine pyrochat-echol)	TMAH (tetramethyl-ammonium hydroxide)	XeF_2	SF_6 Plasma	DRIE (Deep Reactive Ion Etch)
Etch Type	wet	wet	wet	wet	dry	dry	dry
Anisotropic?	no	yes	yes	yes	no	varies	yes
Availability	common	common	moderate	moderate	limited	common	limited
Si Etch Rate µm/min	1 to 3	1 to 2	1 to 30	≈ 1	1 to 3	≈ 1	> 1
Si Roughness	low	low	low	variable	high	variable	low
Nitride Etch	low	low	low	1 to 10 nm/min	?	low	low
Oxide Etch	10 to 30 nm/min	1 to 10 nm/min	1 to 80 nm/min	≈ 1 nm/min	low	low	low
Al Selective	no	no	no	yes	yes	yes	yes
Au Selective	likely	yes	yes	yes	yes	yes	yes
p++ Etch Stop?	no (n slows)	yes	yes	yes	no	no (some dopant effects)	no
Electrochemical Stop?	?	yes	yes	yes	no	no	no
CMOS Compatible?	no	no	yes	yes	yes	yes	yes
Cost	low	low	moderate	moderate	moderate	high	high
Disposal	low	easy	difficult	moderate	N/A	N/A	N/A
Safety	moderate	moderate	low	high	moderate?	high	high

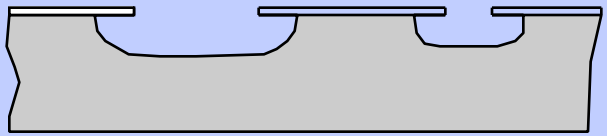
1. Sublimation from solid source.
2. Varies with wt% TMAH, can be controlled to yield very low roughness.
3. Addition of Xe to vary stoichiometry in F or Br etch systems can yield optically smooth surfaces.
4. Some formulations do not attack Al, but are not common.
5. With added Si, polysilicic acid or pH control.
6. Defined as 1) allowing wafer to be immersed directly with no special measures and 2) no alkali ions.
7. Includes cost of equipment.

ISOTROPIC VS. ANISOTROPIC WET ETCHING

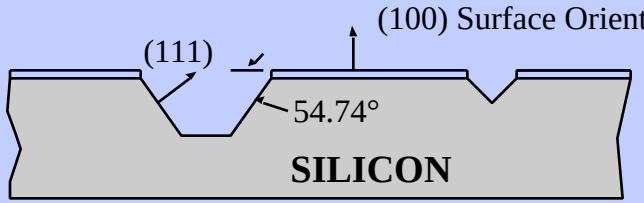
ISOTROPIC WET ETCHING: AGITATION



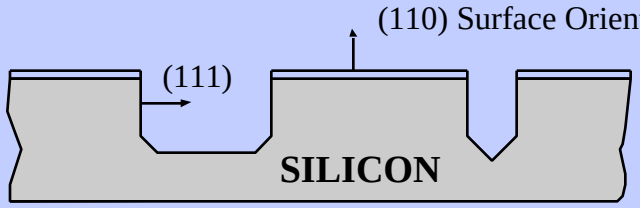
ISOTROPIC WET ETCHING: NO AGITATION



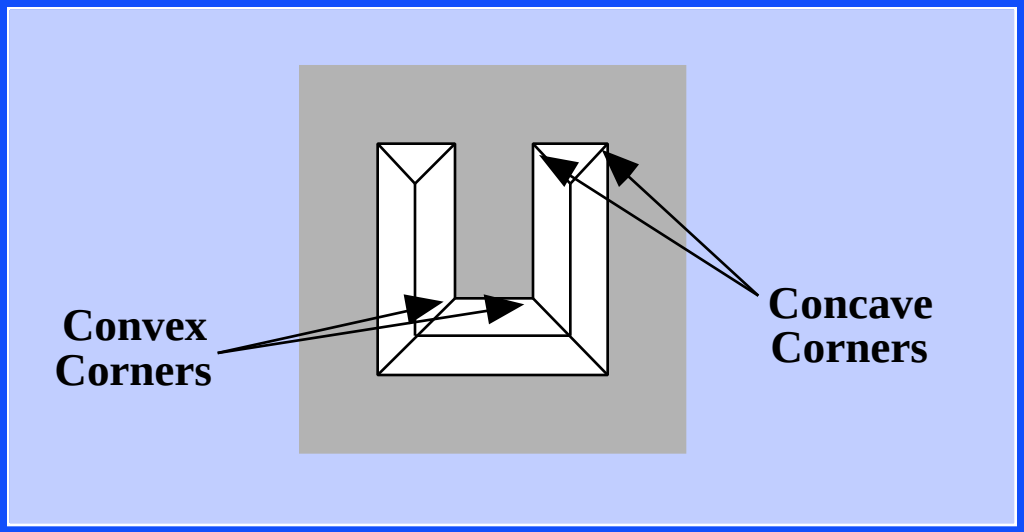
ANISOTROPIC WET ETCHING: (100) SURFACE



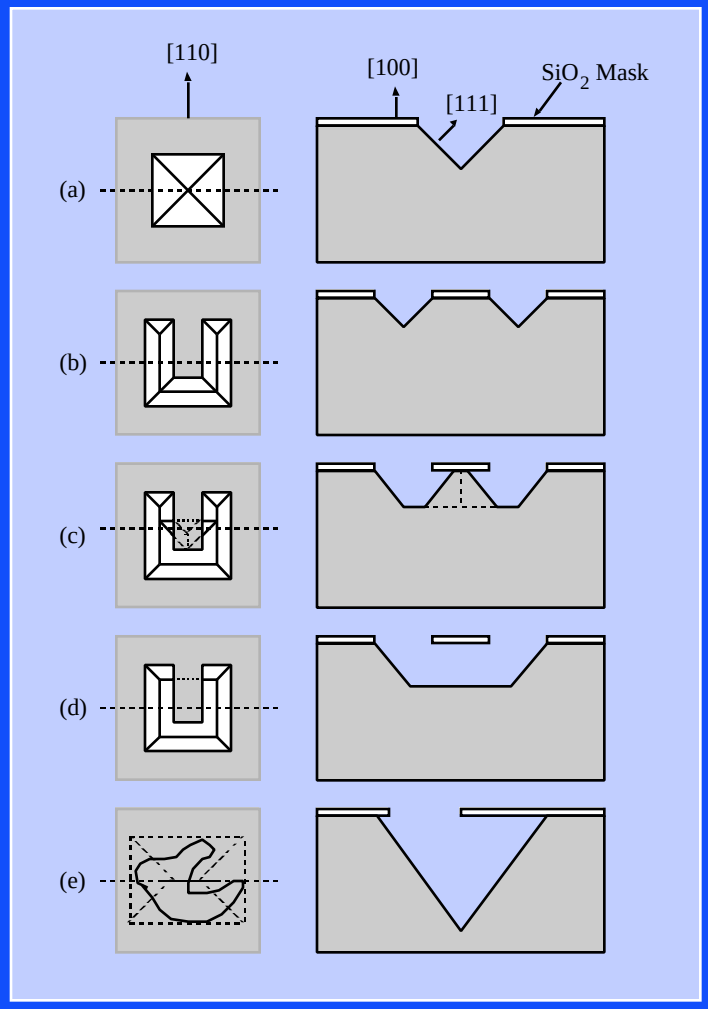
ANISOTROPIC WET ETCHING: (110) SURFACE

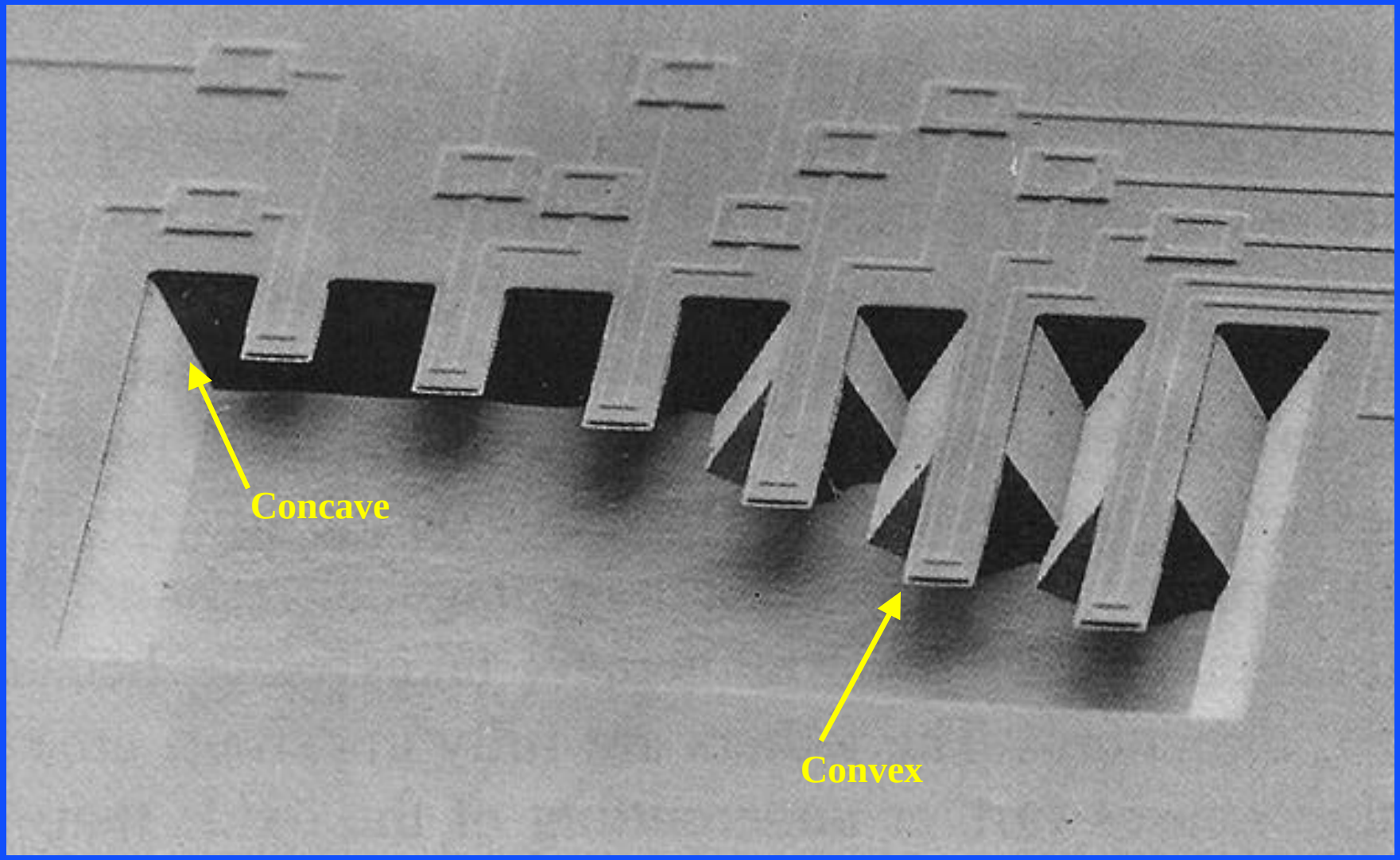


THE IMPORTANCE OF CORNERS IN ANISOTROPIC WET ETCHING

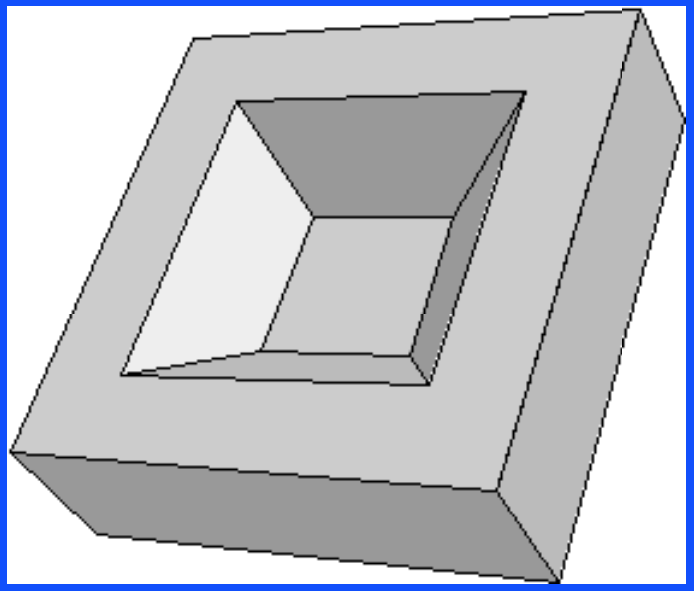


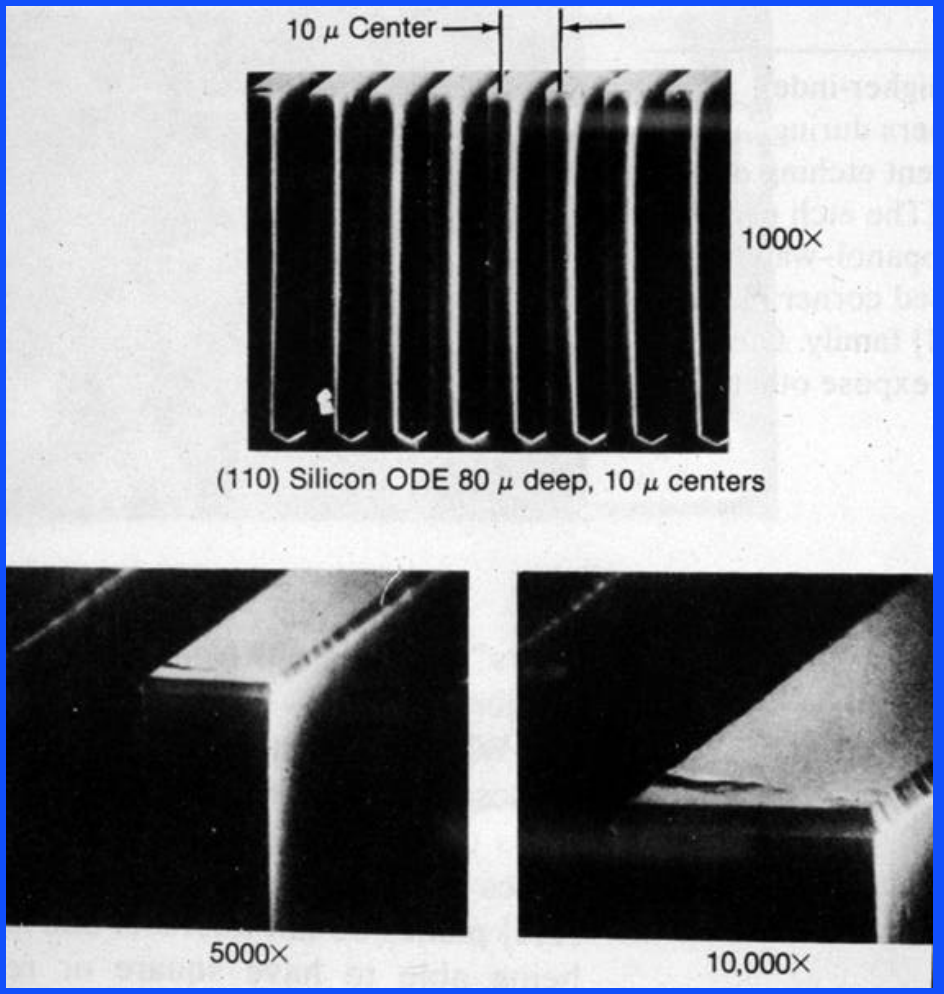
- **Convex corners are undercut.**
- **Concave corners stop at (111) intersections.**

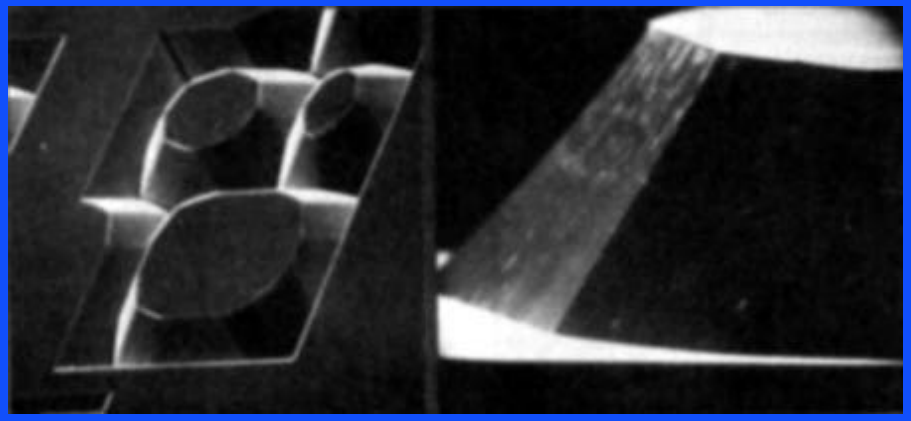




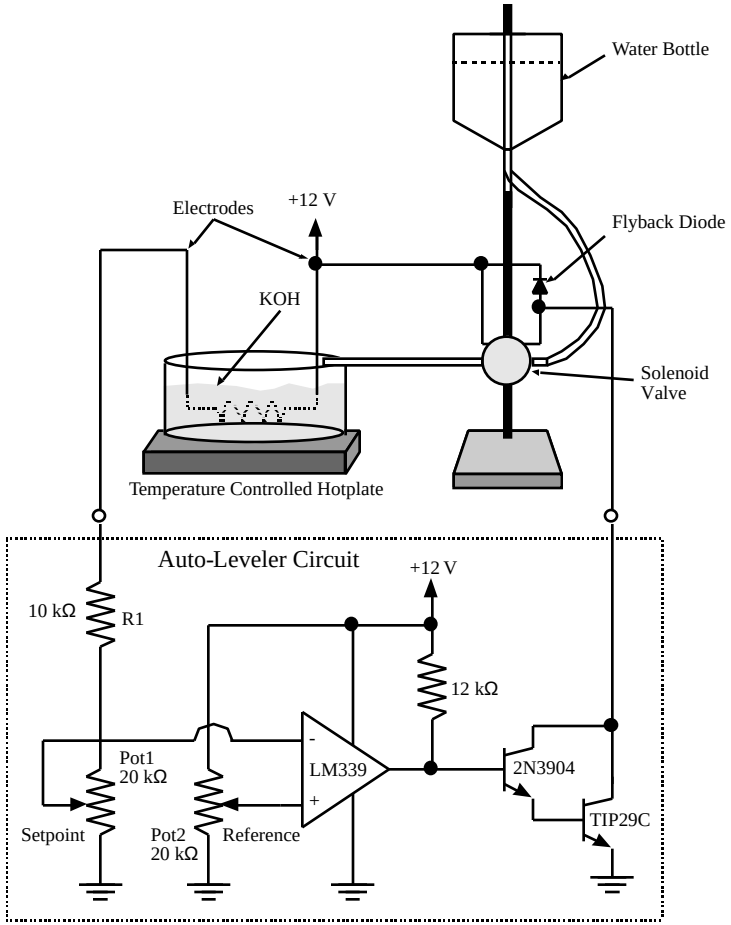
Courtesy Dr. L. Ristic, Motorola, Inc.

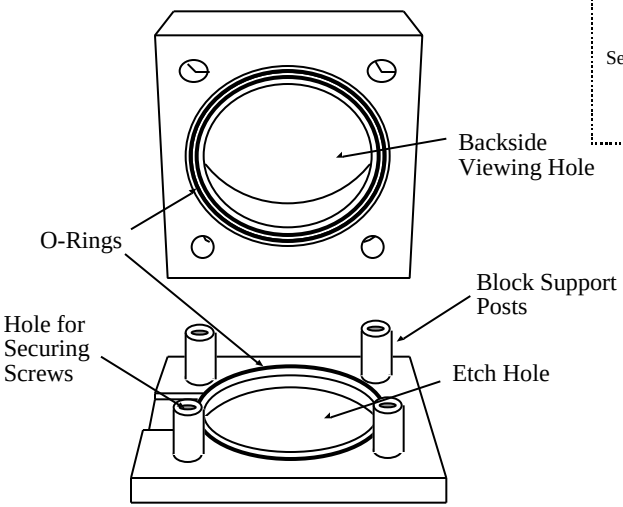




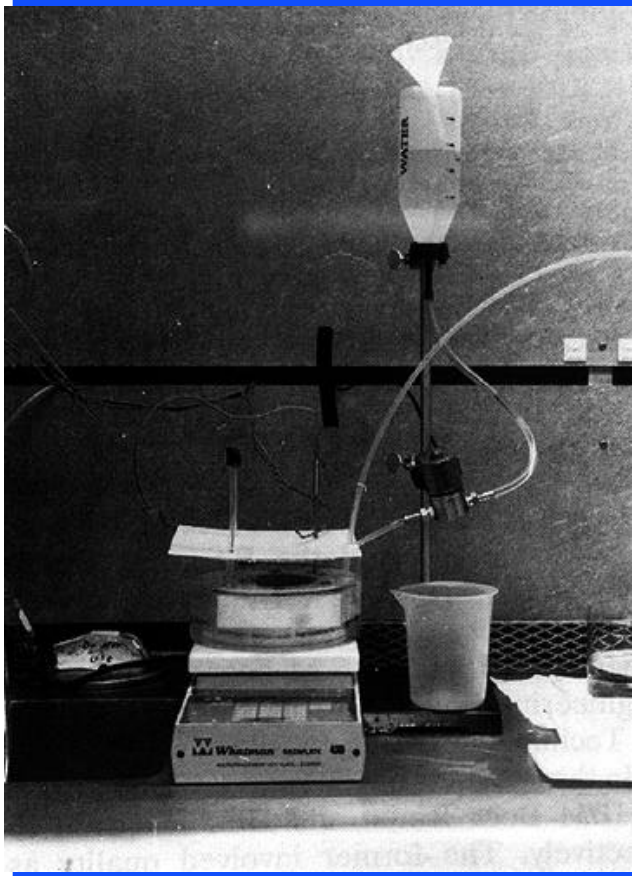


Source of images: Runyan, W. R., and Bean, K. W., "Semiconductor Integrated Circuit Processing Technology," Addison-Wesley, 1990.





One-sided etch apparatus, after Kung, et al. (1991).



ANISOTROPIC SILICON ETCHANTS

- **Alkali hydroxides (KOH, NaOH, etc.): very smooth walls, can use isopropyl alcohol to increase selectivity (111) vs. (100), attacks aluminum, oxide etches somewhat, nitride good mask.**
- **Ethylene Diamine Pyrochatechol (EDP): similar to KOH but much more toxic, does not attack metals (even Al in some cases) nor oxide.**
- **Tetramethyl Ammonium Hydroxide (TMAH): similar to EDP but safer, in some cases will not attack Al, can be masked with oxide.**
- **Amine Gallates: similar to EDP but somewhat safer, not commonly used.**

MECHANISM OF WET ANISOTROPIC SILICON ETCHANTS

1) Injection of holes into the Si to form Si^{+} (higher oxidation state).

2) Attachment of OH^{-} groups to the Si^{+}.

3) Reaction of the "hydrated" Si with a complexing agent in the solution.

4) Dissolution of the reaction products into the solution.

While the reaction mechanisms have generally been elucidated, the mechanisms of dopant modulation and anisotropic etching along crystal planes have not been fully explained.

Silicon atoms at surface react with hydroxyl ions. The silicon is oxidized and four electrons are injected from each silicon atom into the conduction band.

$$Si + 2OH^- \rightarrow Si(OH)_2^{2+} + 4e^-$$

or

$$Si + 2OH^- + 4h^+ \rightarrow Si(OH)_2^{2+}$$

Simultaneously, water is reduced, leading to the evolution of hydrogen.

$$4H_2O + 4e^- \rightarrow 4OH^- + 2H_2$$

or

$$4H_2O \rightarrow 4OH^- + 2H_2 + 4h^+$$

The complexed silicon, $Si(OH)_2^{2+}$, further reacts with hydroxyl ions to form a soluble silicon complex and water.

$$Si(OH)_2^{2+} + 4OH^- \rightarrow SiO_2(OH)_2^{2+} + 2H_2O$$

The overall reaction is,

$$Si + 2OH^- + 2H_2O \rightarrow Si(OH)_2^{2+} + 2H_2$$

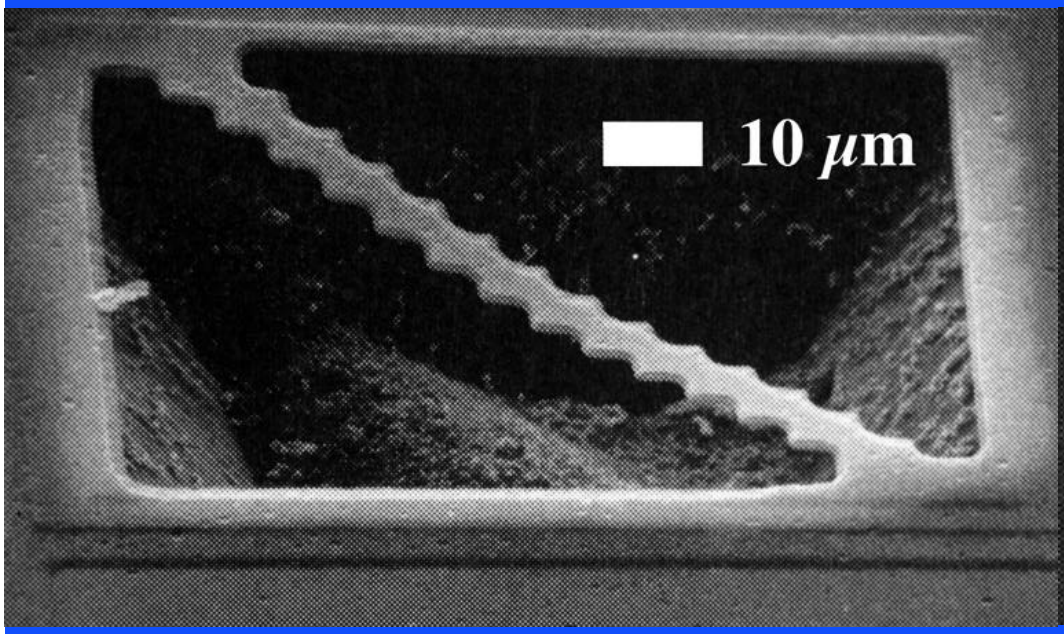
EXAMPLE KOH FORMULATIONS

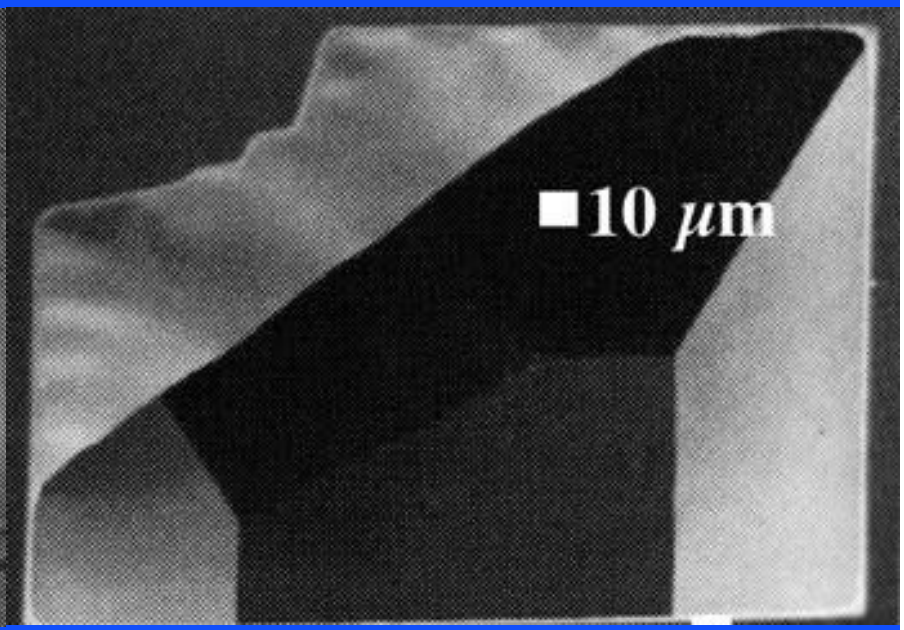
Formulation	Temp °C	Etch Rate (μm/min)	(100)/(111) Etch Ratio	Masking Films (etch rate)
KOH (44 g) Water, Isopropanol (100 ml)	85	1.4	400:1	SiO_2 (1.4 nm/min) Si_3N_4 (negligible)
KOH (50 g) Water, Isopropanol (100 ml)	50	1.0	400:1	approx. as above
KOH (10 g) Water (100 ml)	65	0.25 to 1.0	-	SiO_2 (0.7 nm/min) Si_3N_4 (negligible)

EXAMPLE EDP FORMULATIONS

Formulation	Temp °C	Etch Rate (μm/min)	(100)/(111) Etch Ratio	Masking Films (etch rate)
Ethylene diamine (750 ml) Pyrocatechol (120 g) Water (100 ml)	115	0.75	35:1	SiO_2 (0.2 nm/min) Si_3N_4 (0.1 nm/min) Au, Cr, Ag, Cu, Ta (negligible)
Ethylene diamine (750 ml) Pyrocatechol (120 g) Water (240 ml)	115	1.25	35:1	as above

EDP RESIDUE REMOVAL WITH ASCORBIC ACID



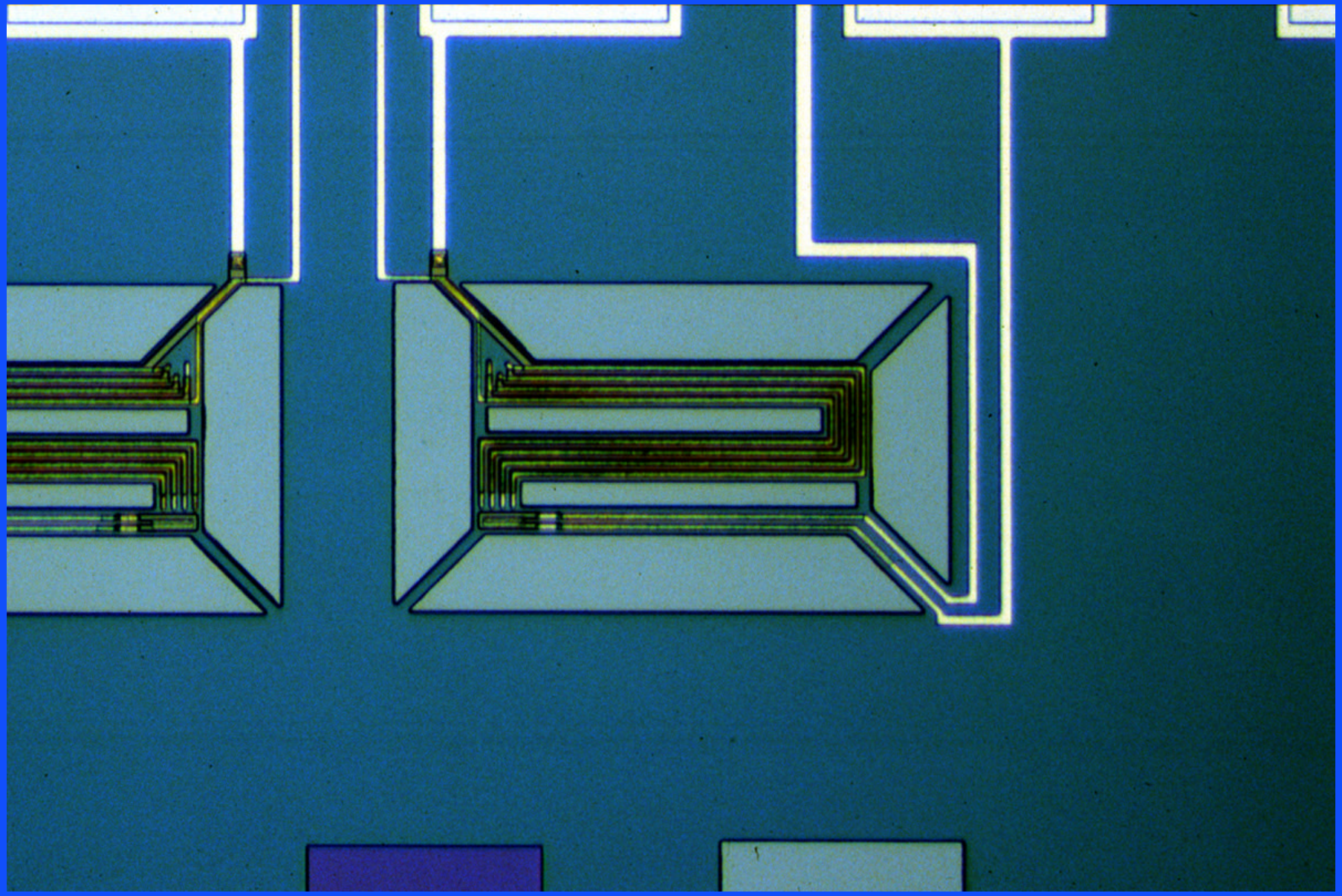


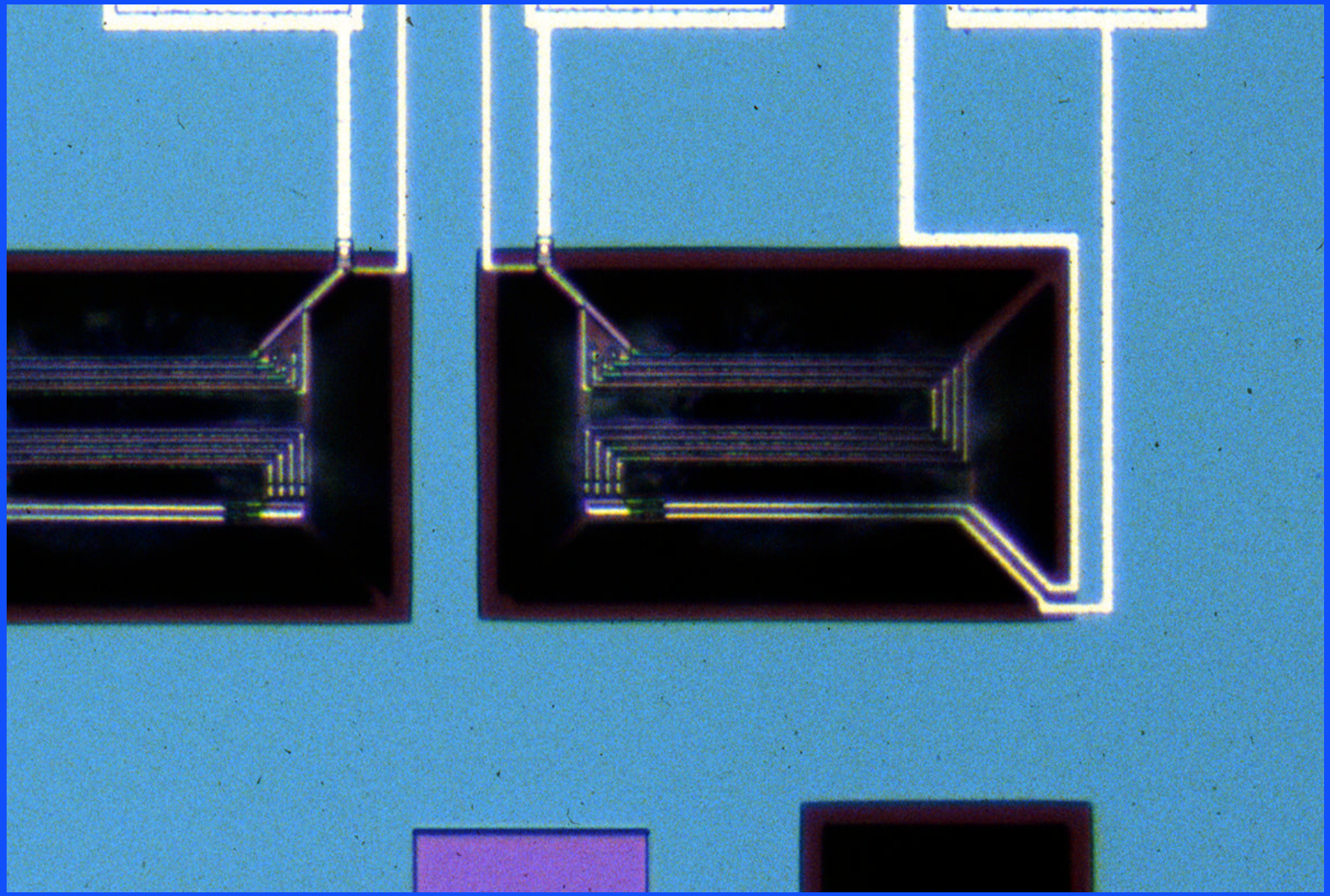
Source: Dr. D. Moser, Doctoral Thesis, ETH Zurich.

TMAH SELECTIVITY

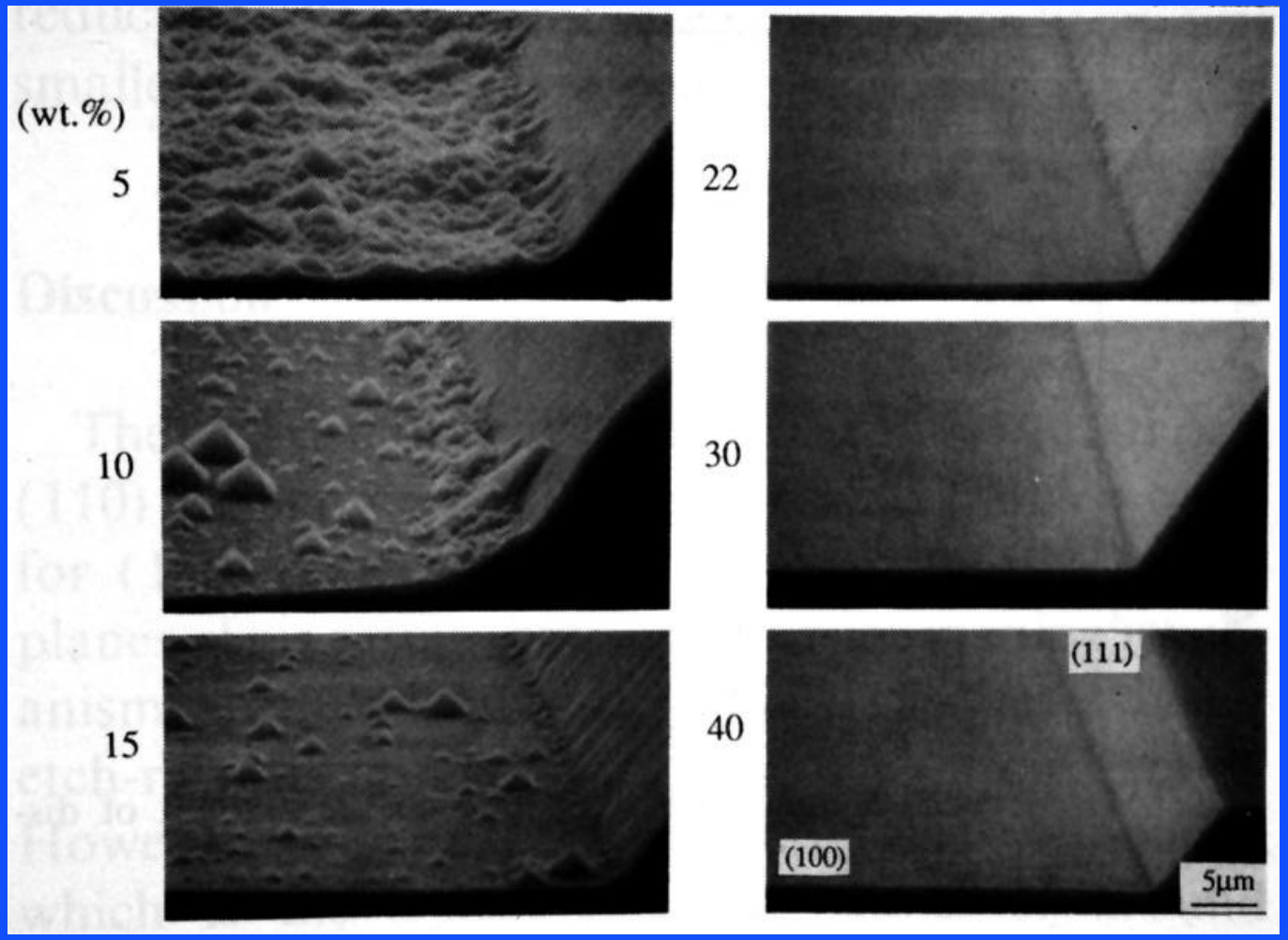
Selectivity of TMAH Etchants for Various Dielectrics versus (100) Silicon

Dielectric	Selectivity 4 wt% TMAH, 80°C	Selectivity (Si-doped, 13.5g/l), 4 wt% TMAH, 80°C	Selectivity 20 wt% TMAH, 95°C
Thermal Silicon Dioxide	5.3×10^3	34.7×10^3	5.2×10^3
Low-Temperature Oxide (LTO)	1.3×10^3	4.2×10^3	2.8×10^3 (360° LTO) 3.4×10^3 (360° LTO)
PECVD Oxide	1.4×10^3	4.3×10^3	no value given
LPCVD Silicon Nitride	24.4×10^3	49.3×10^3	38×10^3
PECVD Silicon Nitride	9.2×10^3	18.5×10^3	3.6×10^3
Source	Schnakenberg, et al. (1991)	Schnakenberg, et al. (1991)	Ristic, et al. (1994)





TMAH ETCH ROUGHNESS



Data for 90 min. etches at 70°C.

Source: Tabata, O., Asahi, R., Funabashi, H., and Sugiyama, S., "Anisotropic Etching of Silicon in $(CH_3)_4NOH$ Solutions," Proceedings of Transducers '91, San Francisco, CA, June 24 - 27, 1991, pp. 811 - 814.

WHY ETCHING SLOWS ON (111) PLANES

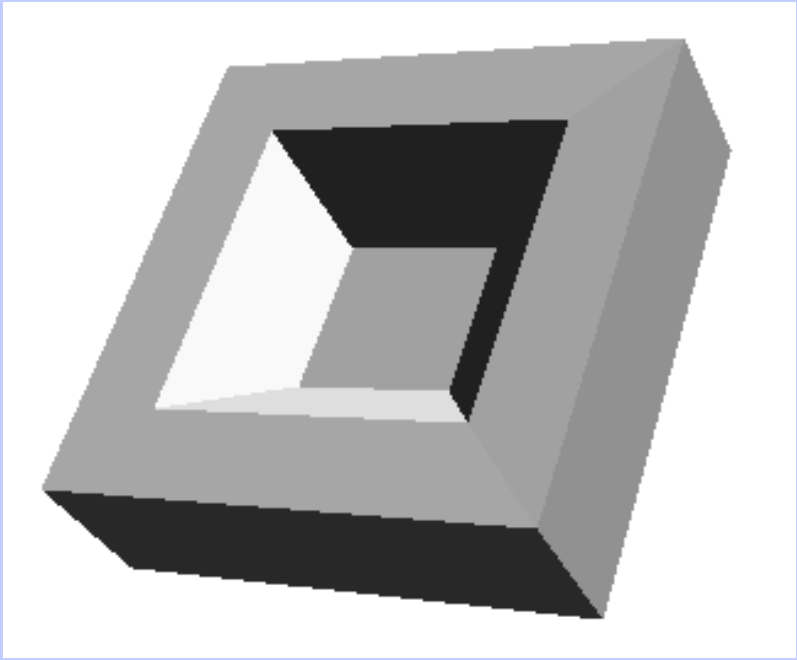
- For KOH the relative etch rates are: (111) (reference) = 1, (100) = 300 - 400, (110) = 600.

- The main reason that the (111) planes of Si are so chemically passive is that on this plane the bonds of neighboring Si atoms (purely covalent, based on overlaps of four sp^3 hybridized molecular orbitals) are perpendicular to the (111) plane (on alternate atomic layers), with full rotational symmetry about the perpendicular axis.

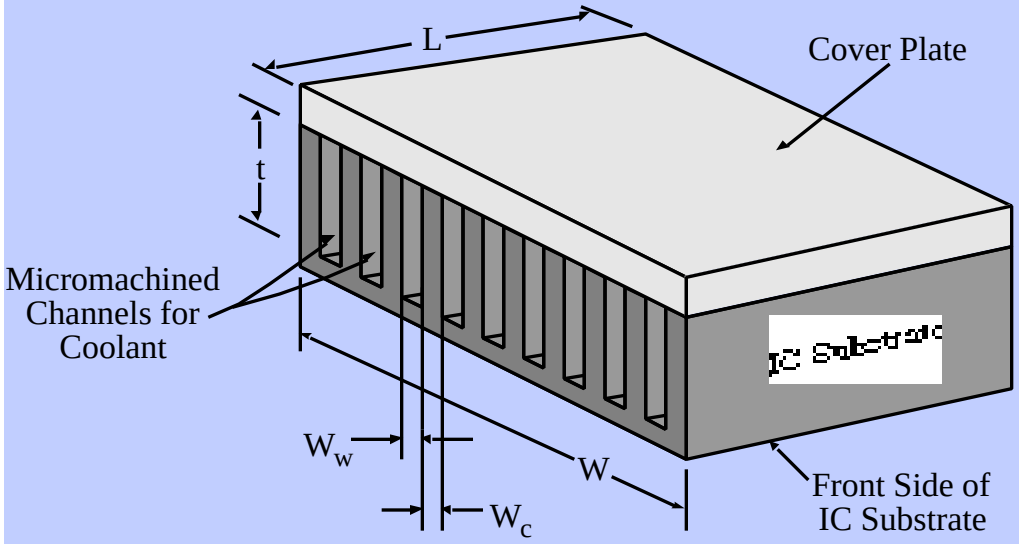
- An sp^3 hybrid orbital pointing out perpendicular to the (111) plane can only bond with another perpendicularly-oriented sp^3 or a solitary s orbital (e.g. hydrogen atom), excluding p_x, p_y, and p_z orbitals due to symmetry restrictions.

- On (100) and (110) planes, the sp^3 orbitals emerge from the plane surfaces well away from perpendicular and thus able to react (form "nonzero overlap integrals") with any available p_x, p_y, or p_z orbitals as available in all etchant or oxidizer molecules.

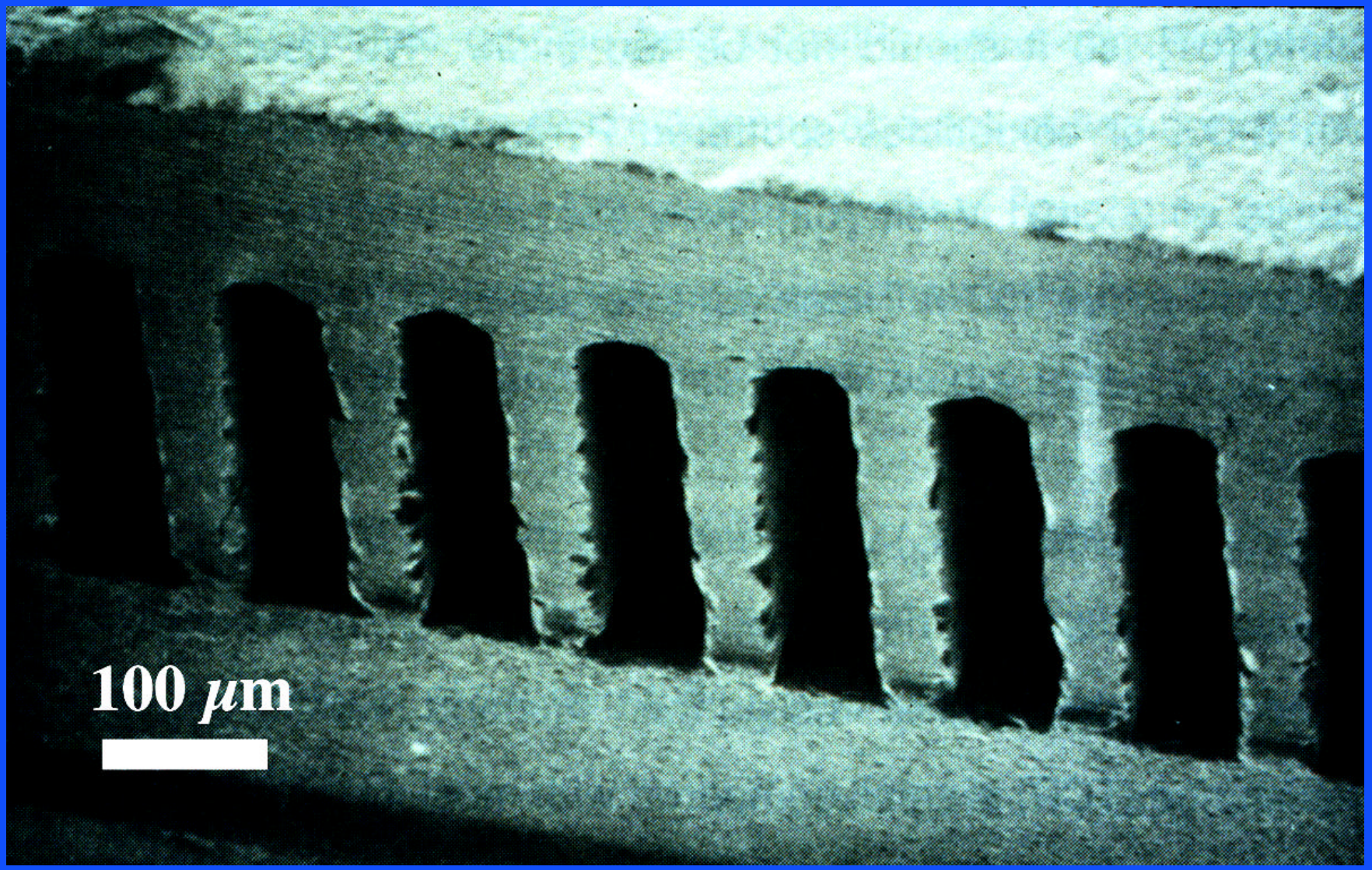
EXAMPLES OF ANISOTROPIC ETCHING



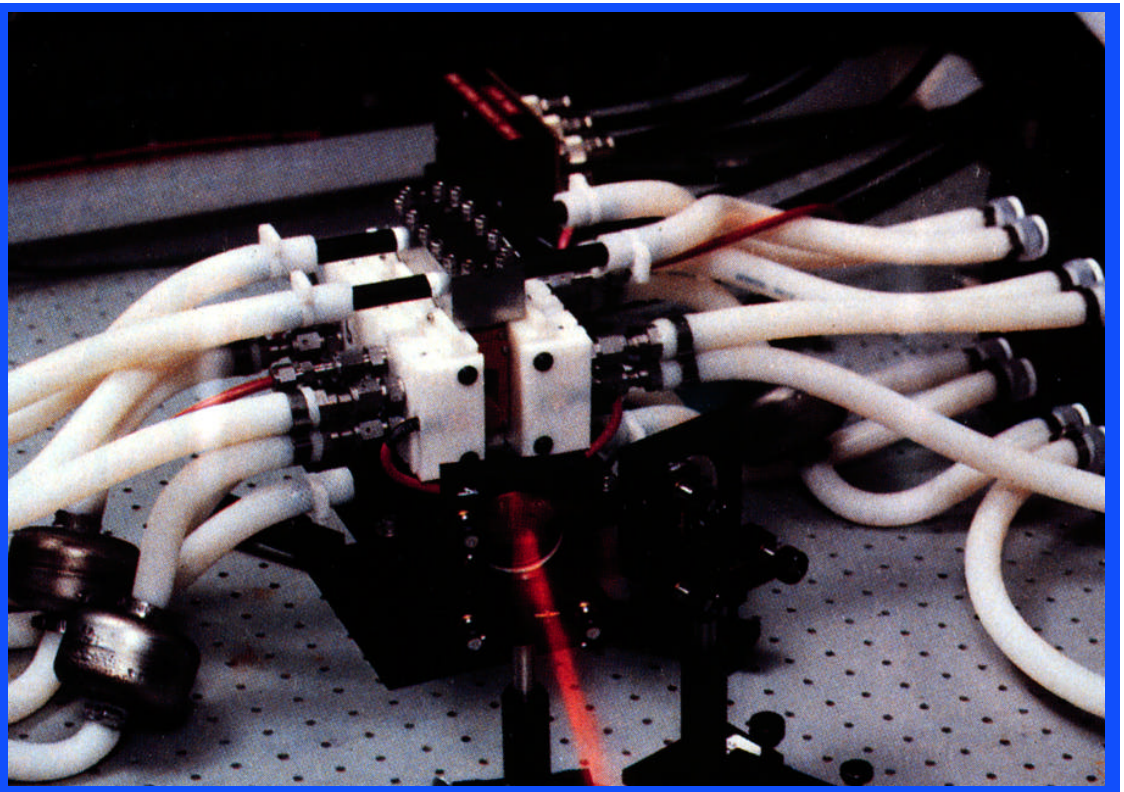
Typical etched pit in silicon.



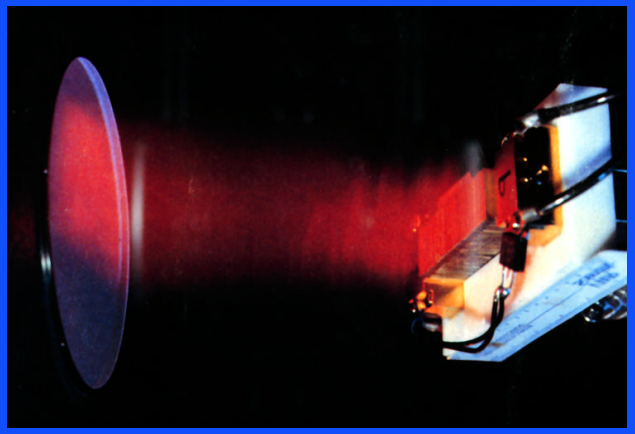
Tuckerman and Pease (110) cooling channels.

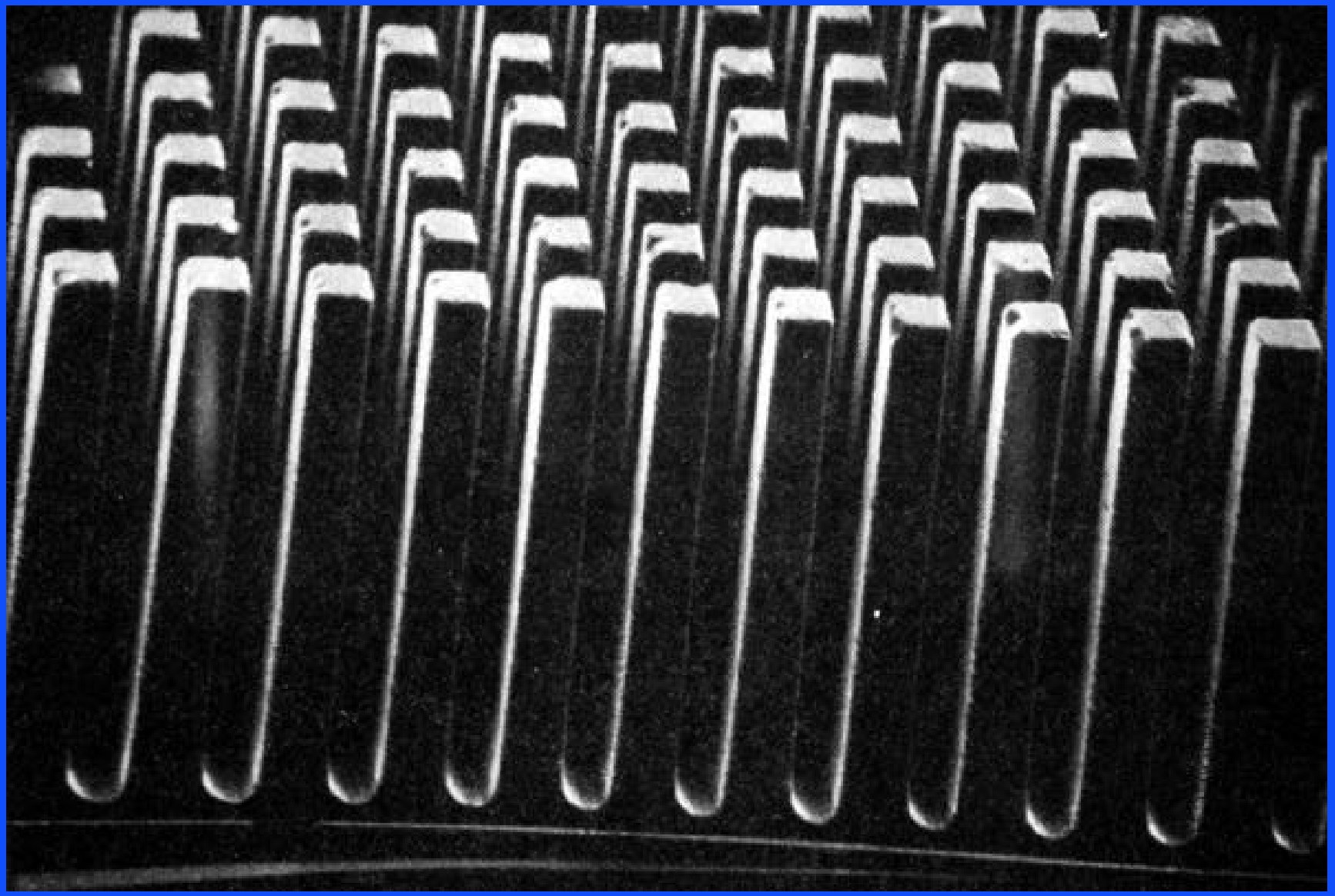


Tuckerman, D. B., and Pease, R. F. W., "High-Performance Heat Sinking for VLSI," IEEE Electron Device Letters, vol. EDL-2, no. 5, May 1981, pp. 126 - 129.



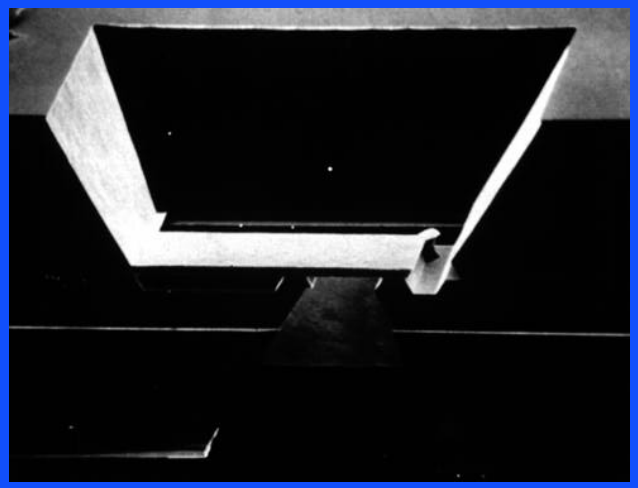
Lawrence Livermore National Laboratory



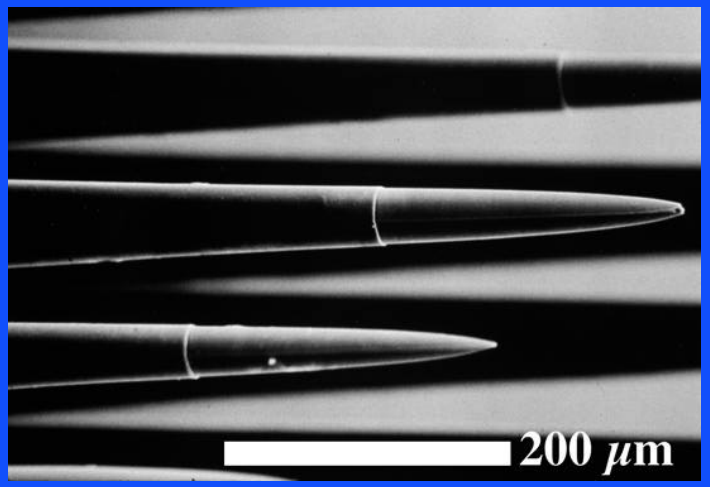


Tuckerman, D. B., and Pease, R. F. W., “High-Performance Heat Sinking for VLSI,” IEEE Electron Device Letters, vol. EDL-2, no. 5, May 1981, pp. 126 - 129.

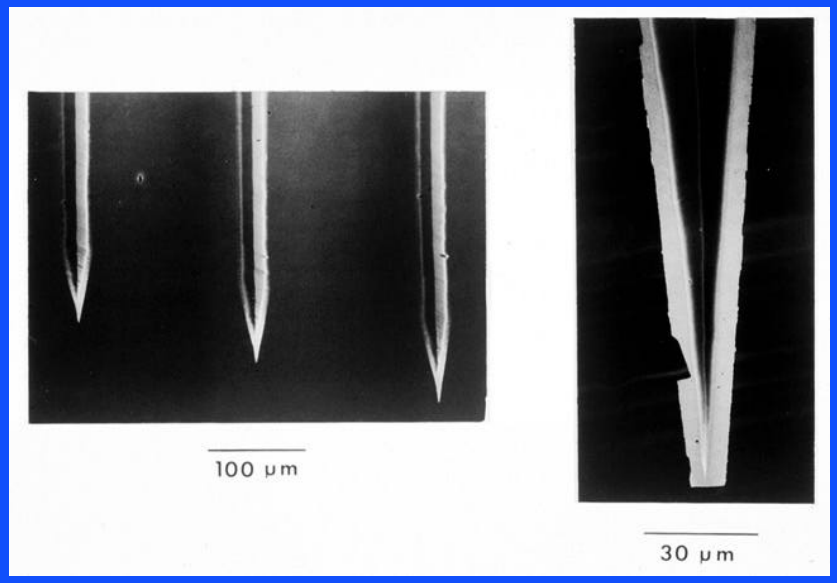
MORE EXAMPLES OF WET ETCHING



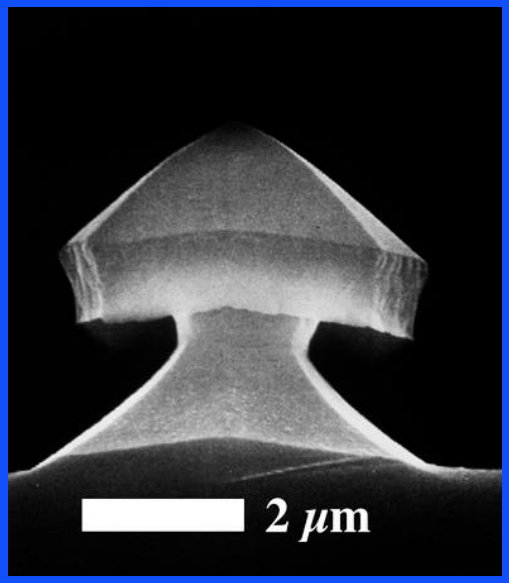
Source: Journal of Micromechanics and Microengineering.



Courtesy Prof. R. Normann, University of Utah.



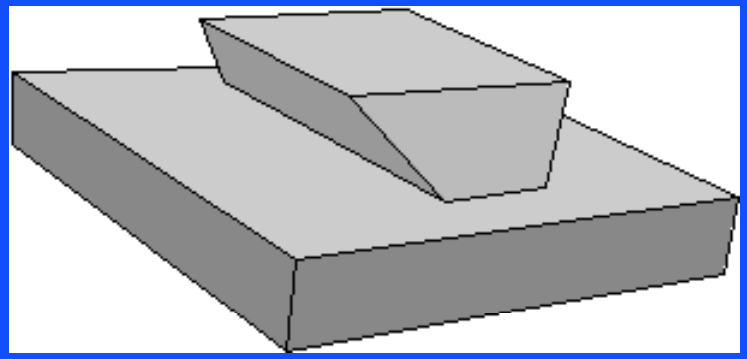
Courtesy Prof. J. Bower, Caltech.



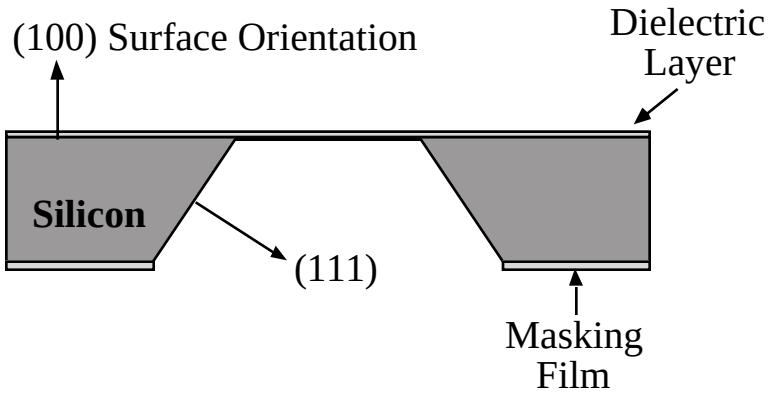
Courtesy Prof. M. Reed, Carnegie Mellon University

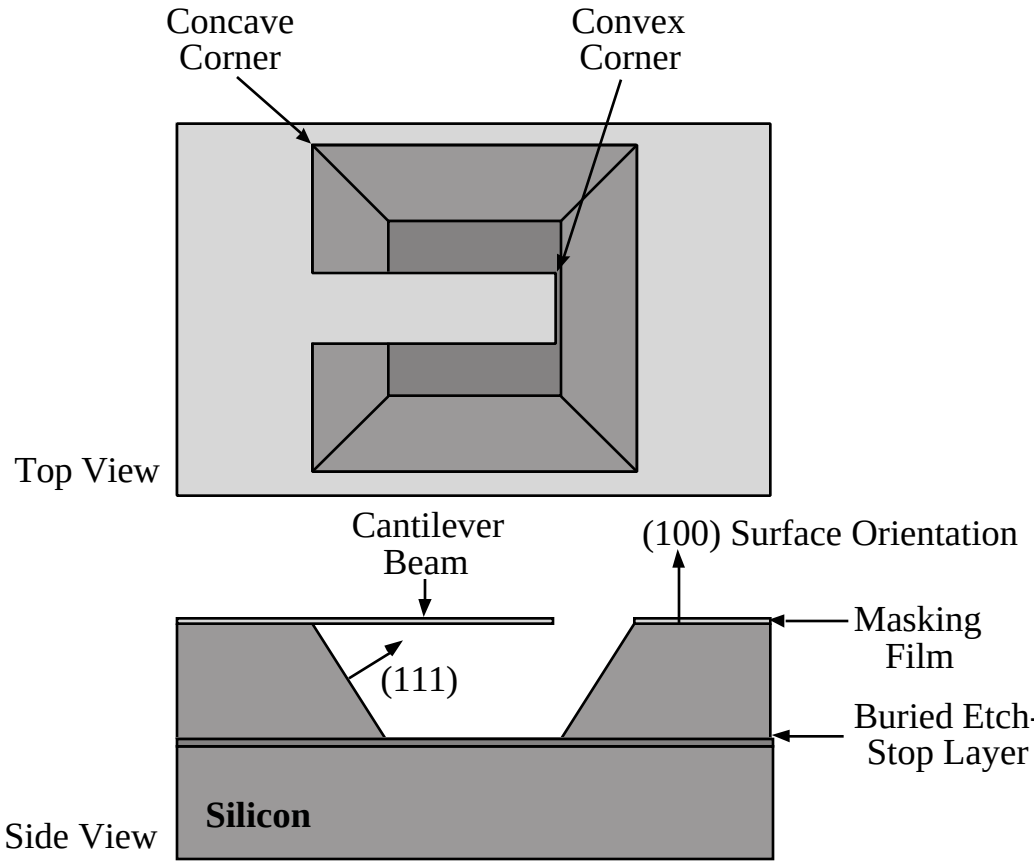
ETCHING III-V COMPOUNDS

- **A variety of shapes not possible in silicon can be obtained through wet etching of III-V compounds.**
- **Typical GaAs etchants are: Br_2:CH_3OH (1:99), H_3PO_4:H_2O_2:CH_3OH (1:1:3) and H_3PO_4:H_2O_2:H_2O (3:1:50), all with different etch properties.**
- **A key feature of GaAs is that it is piezoelectric.**



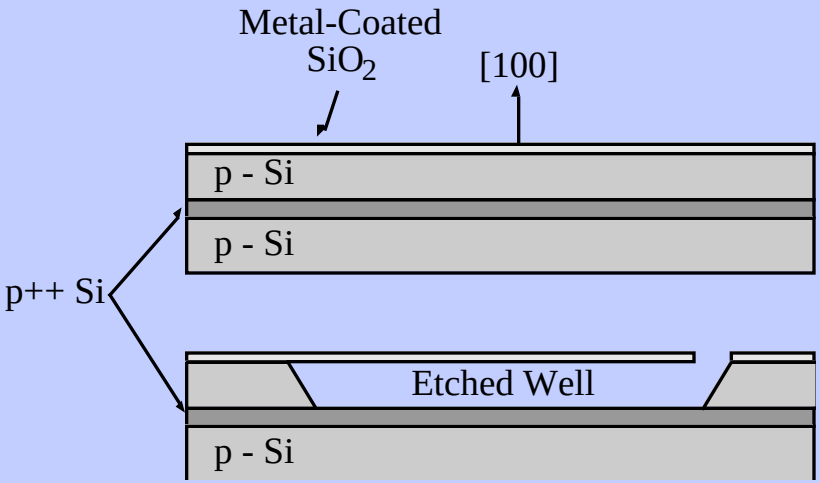
HOW TO MAKE MEMBRANES AND CANTILEVERS



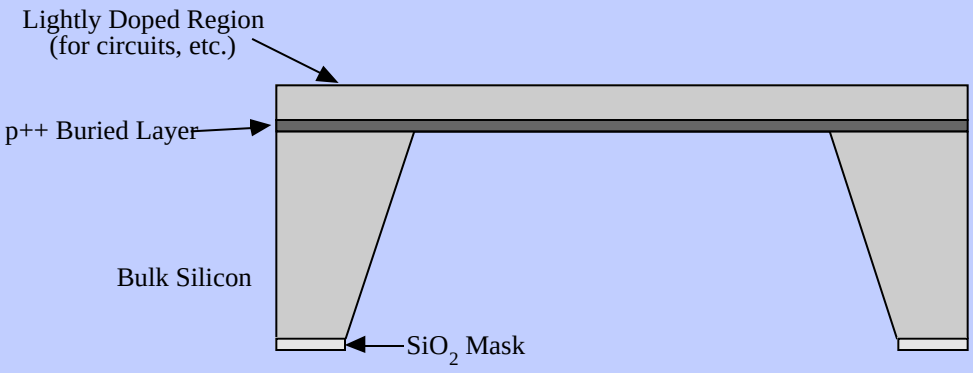


DOPANT ETCH STOPS

- **The anisotropic etchants described slow down markedly at high boron concentrations (≈ 10^{20} cm^{-3}).**
- **Can diffuse (implant?) or grow boron-containing epitaxial silicon.**



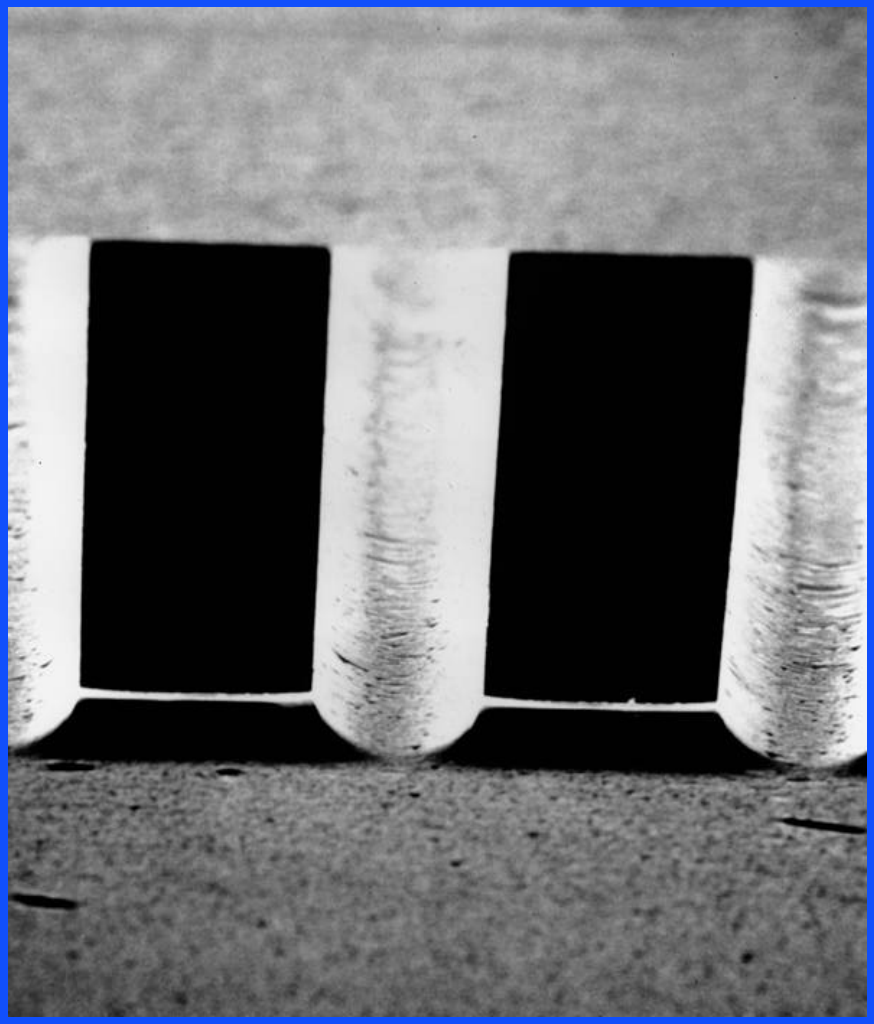
Petersen's method for cantilever fabrication.

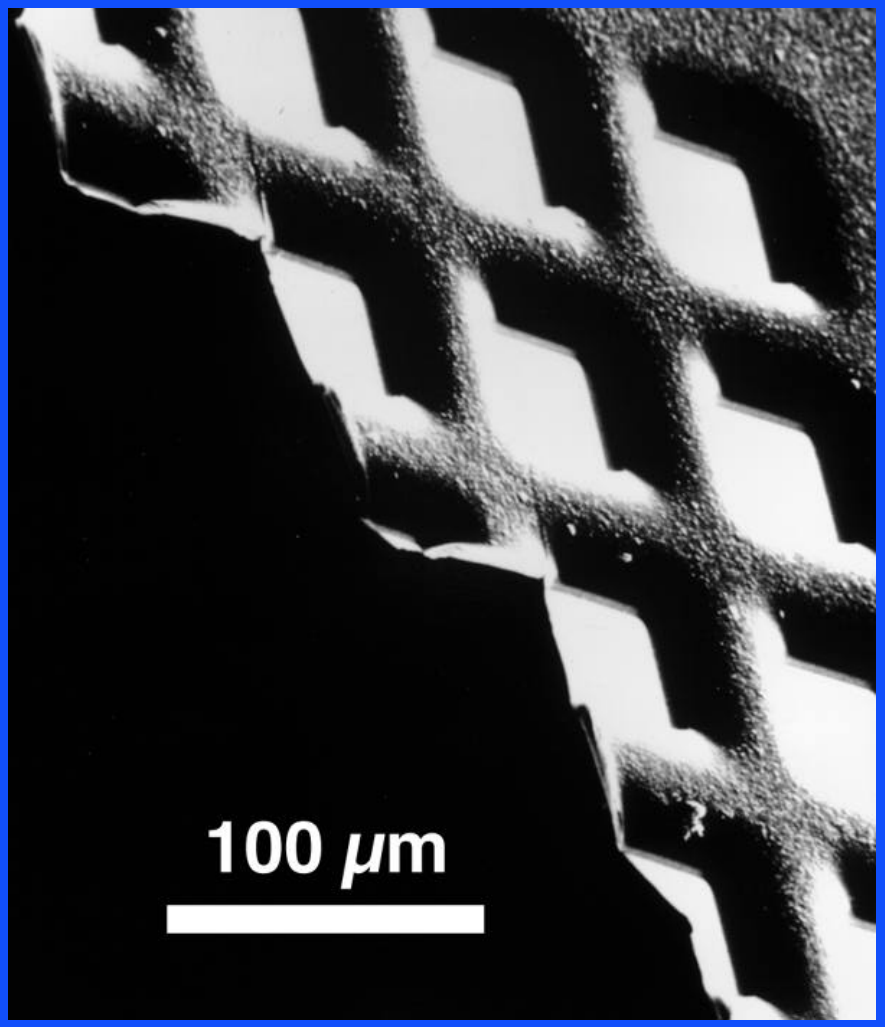


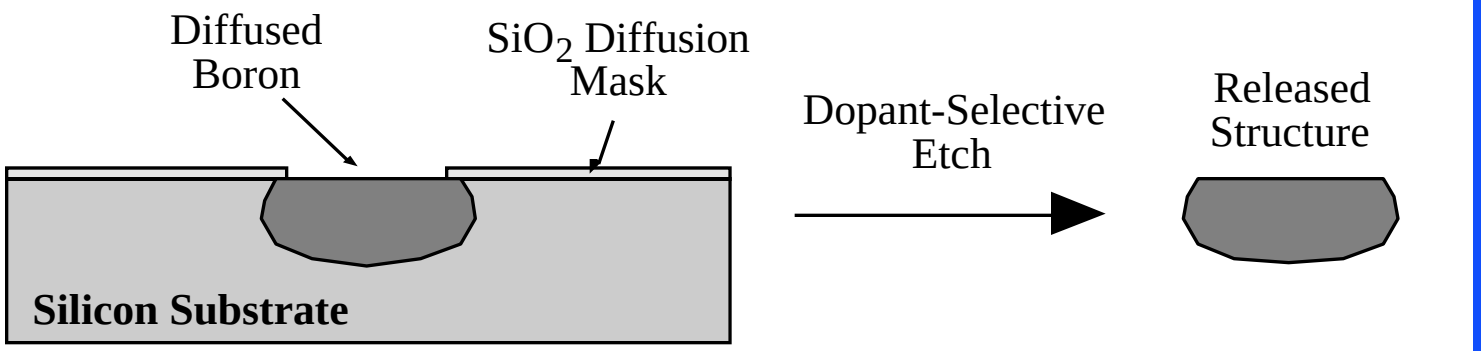
Buried p++ etch stop for membrane formation.

Petersen, K. E., "Dynamic Micromechanics in Silicon: Techniques and Devices," IEEE Transactions on Electron Devices, vol. ED-25, no. 10, Oct. 1978, pp. 1241 - 1250.

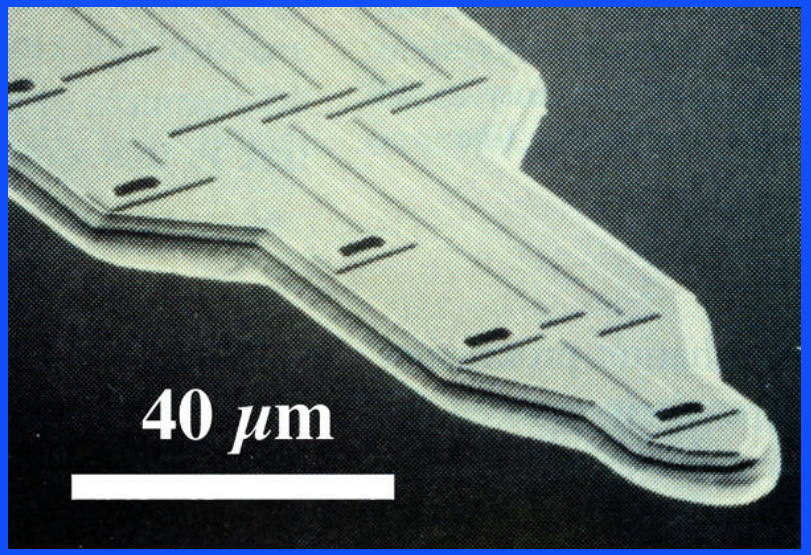
BORON p++ ETCH STOP





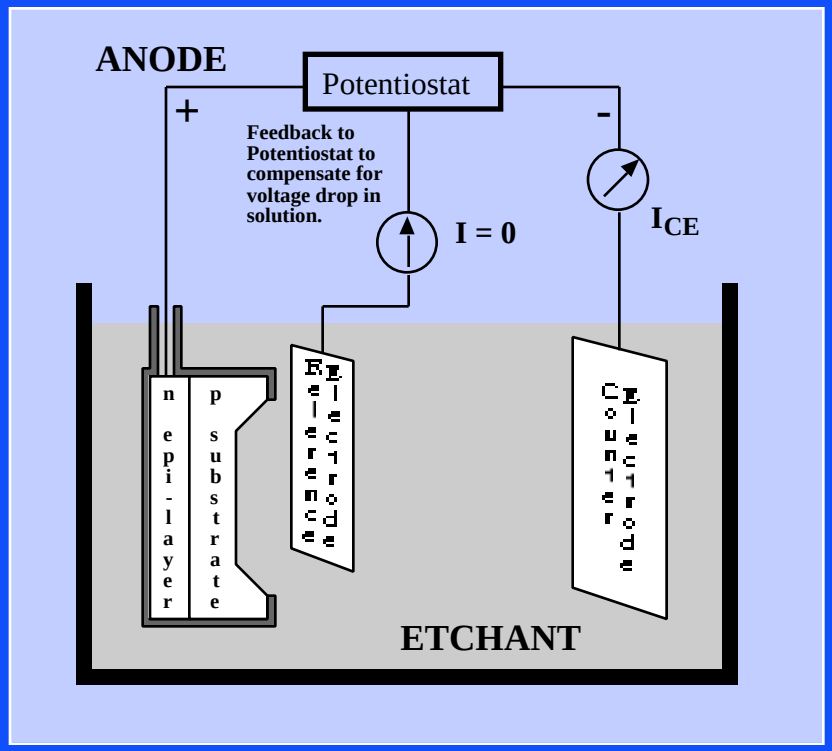


BORON SELECTIVE ETCHING FOR NEURAL PROBES



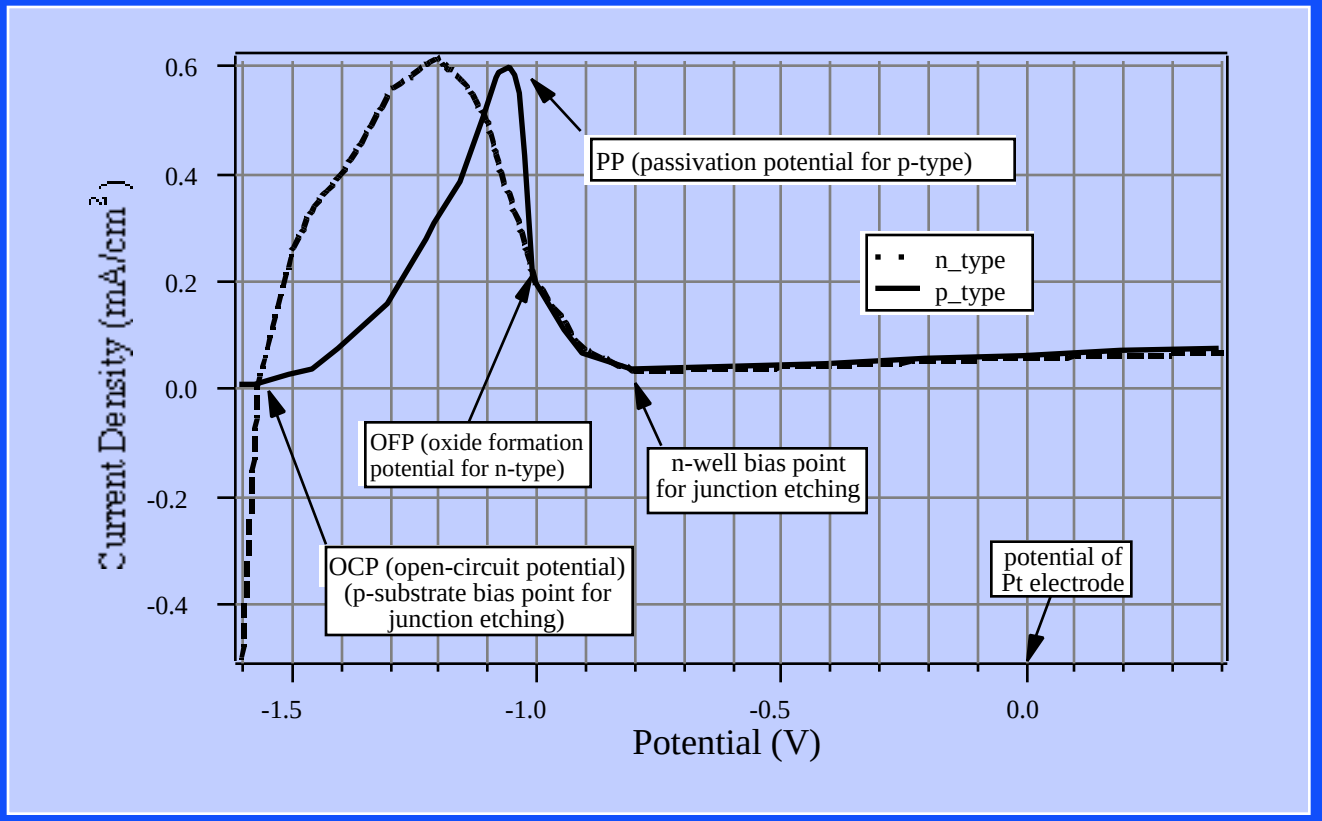
Najafi, K., Wise, K. D., and Mochizuki, T., "A High-Yield IC-Compatible Multichannel Recording Array," IEEE Transactions on Electron Devices, vol. ED-32, no. 7, July 1985, pp. 1206 - 1211.

ELECTROCHEMICAL ETCH STOPS

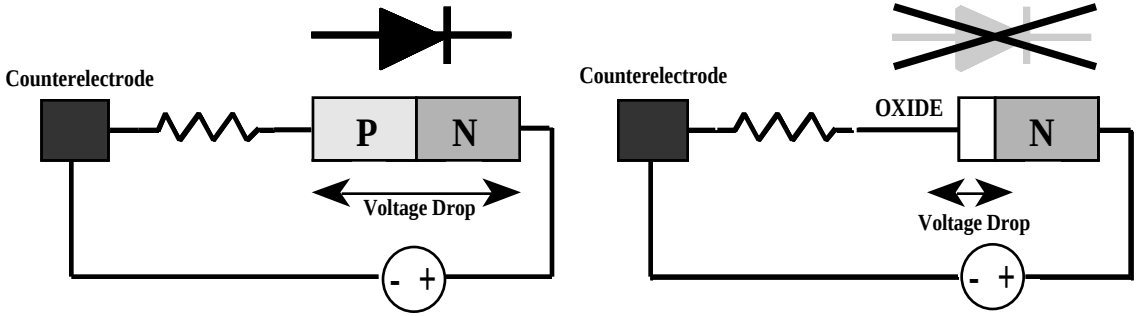


- Can electrochemically modulate silicon etching in HF or KOH-like etchants.
- At sufficiently anodic (positive) potentials, an oxide layer forms on the silicon and etching stops in hydroxide etches (not in HF, where oxide is very soluble, hence electropolishing).
- Can make diode structures that stop etching when the voltage drop is across the n-type material.

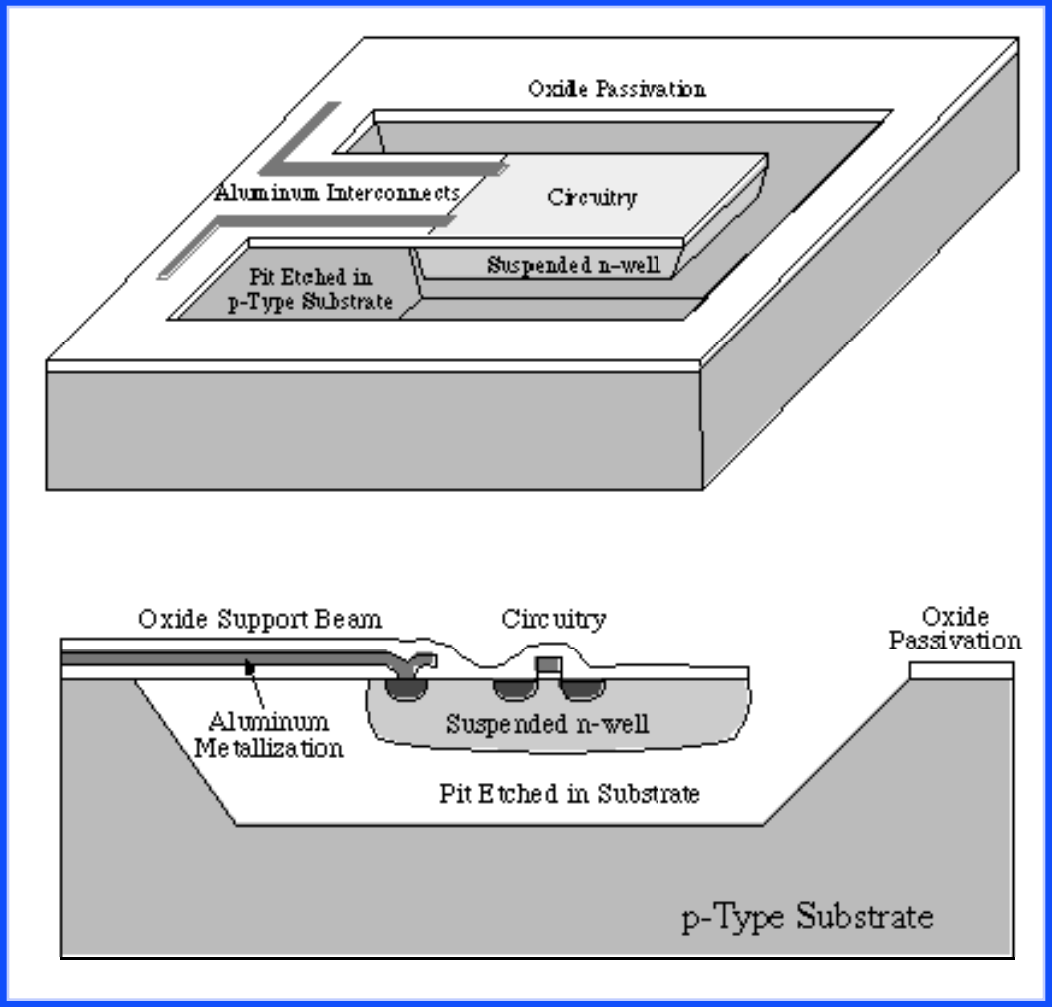
Kloeck, B., Collins, S., de Rooij, N., and Smith, R. L, "Study of Electrochemical Etch-Stop for High-Precision Thickness Control of Silicon Membranes," IEEE Transactions Electron Devices, vol. 36, no. 4, Apr. 1989, pp. 663 - 669.



Kloeck, B., Collins, S., de Rooij, N., and Smith, R. L, "Study of Electrochemical Etch-Stop for High-Precision Thickness Control of Silicon Membranes," IEEE Transactions Electron Devices, vol. 36, no. 4, Apr. 1989, pp. 663 - 669.

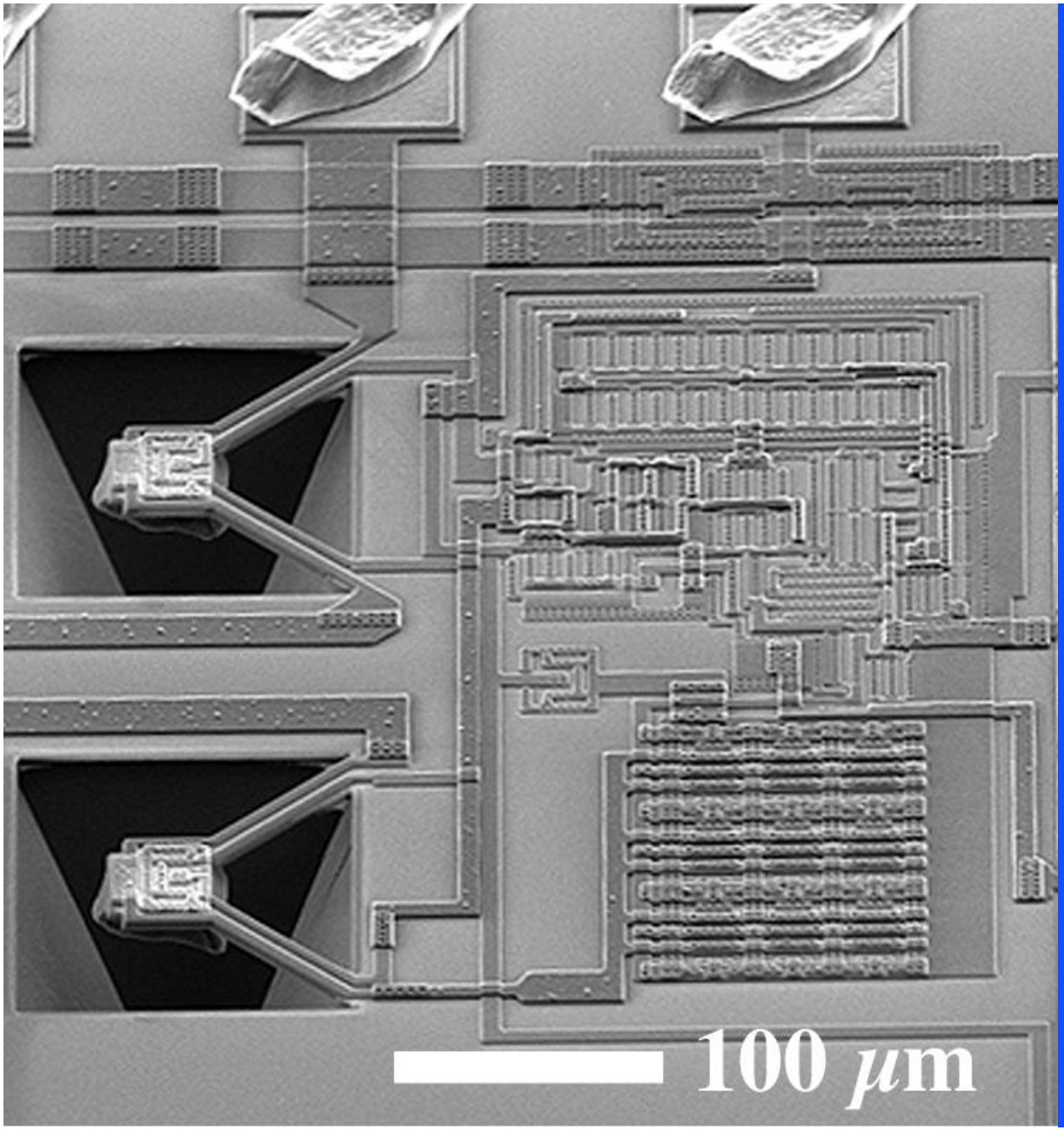


ELECTROCHEMICAL ETCHING n-WELLS IN CMOS



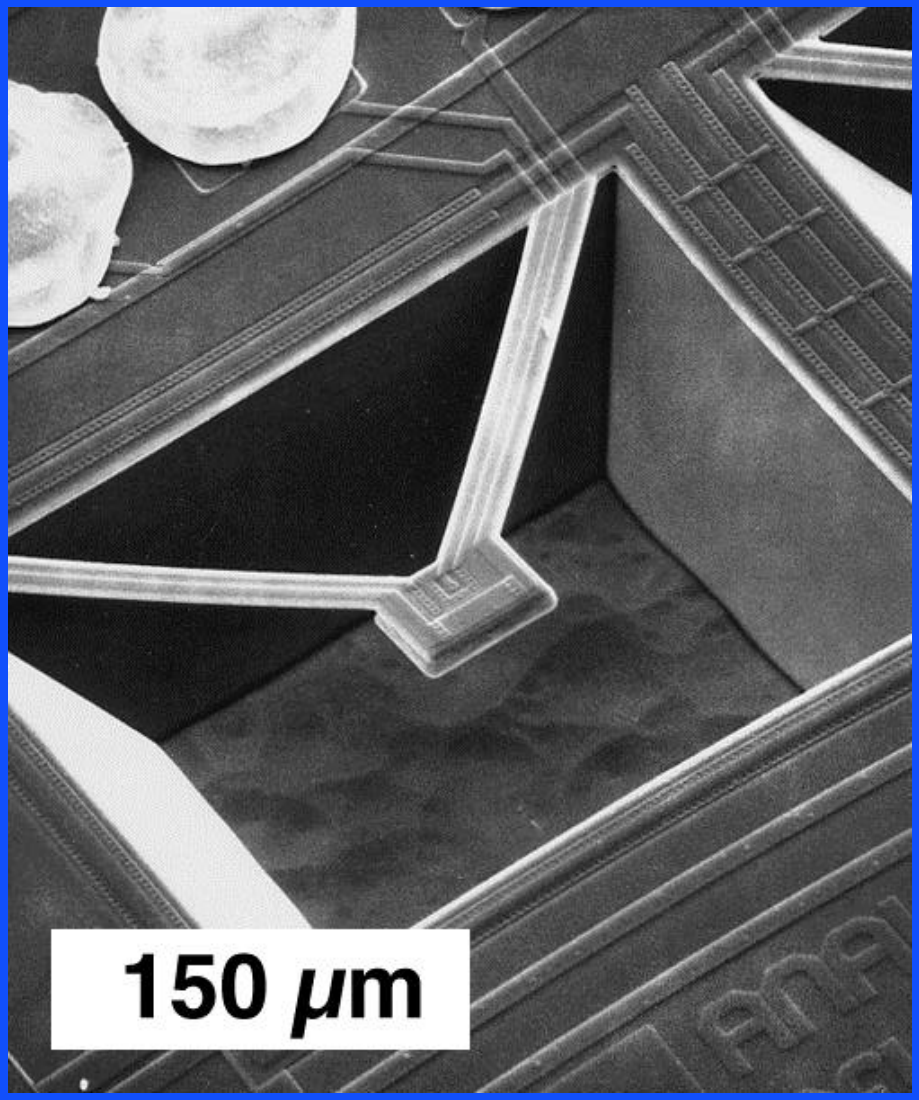
- **Use standard CMOS to form suspended (isolated) single-crystal islands.**
- **Use "open" mask to leave bare silicon regions.**
- **With appropriate TMAH formulation, exposed Al is not attacked.**
- **n-Wells are biased more anodic than passivation potential and are not etched.**

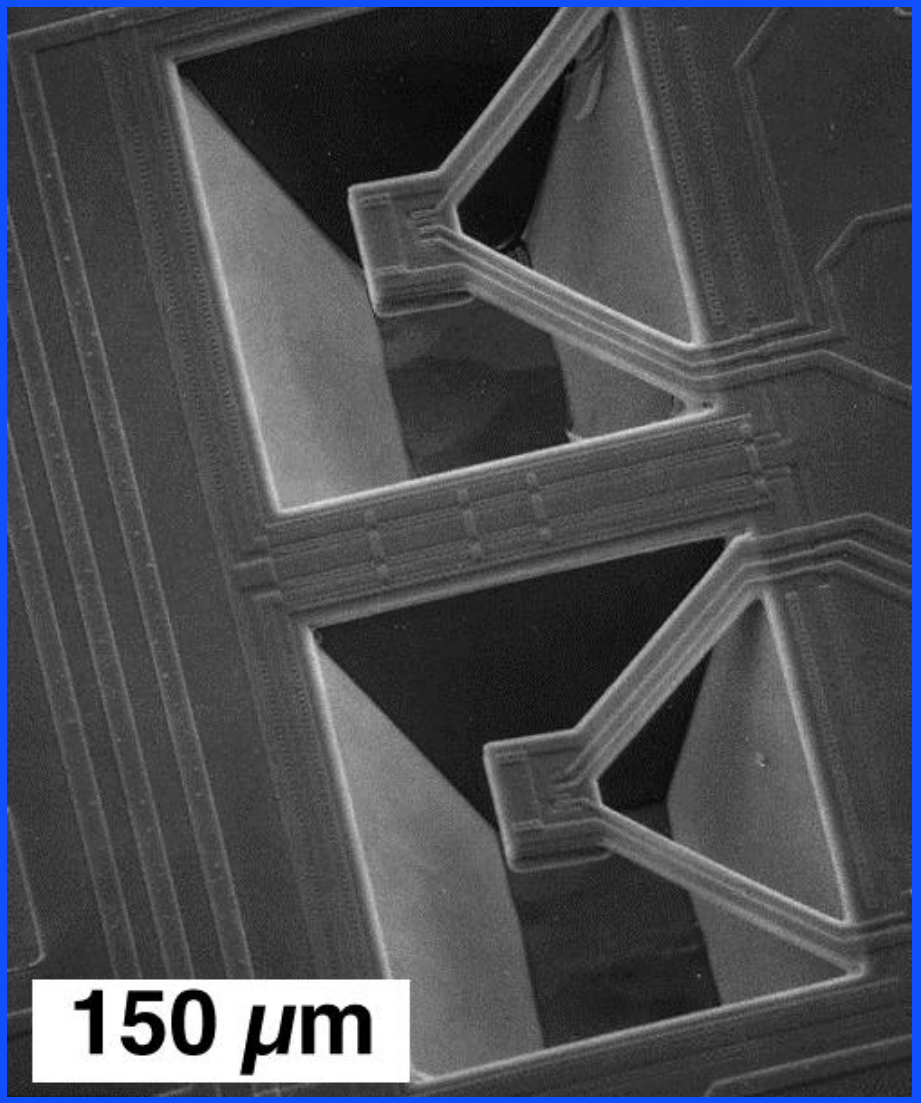
Reay, R. J., Klaassen, E. H. and Kovacs, G. T. A., "Thermally and Electrically Isolated Single-Crystal Silicon Structures in CMOS Technology," IEEE Electron Device Letters, vol. 15, no. 10, Oct. 1994, pp. 399 - 401.



Klaassen, E. H., Reay, R. J., and Kovacs, G. T. A., "Diode-Based Thermal R.M.S. Converter with On-Chip Circuitry Fabricated Using CMOS Technology," Sensors and Actuators, vol. A52, nos. 1 - 3, Mar. - Apr. 1996, pp. 33 - 40.

Courtesy Dr. Erno Klaassen, IBM Corp.

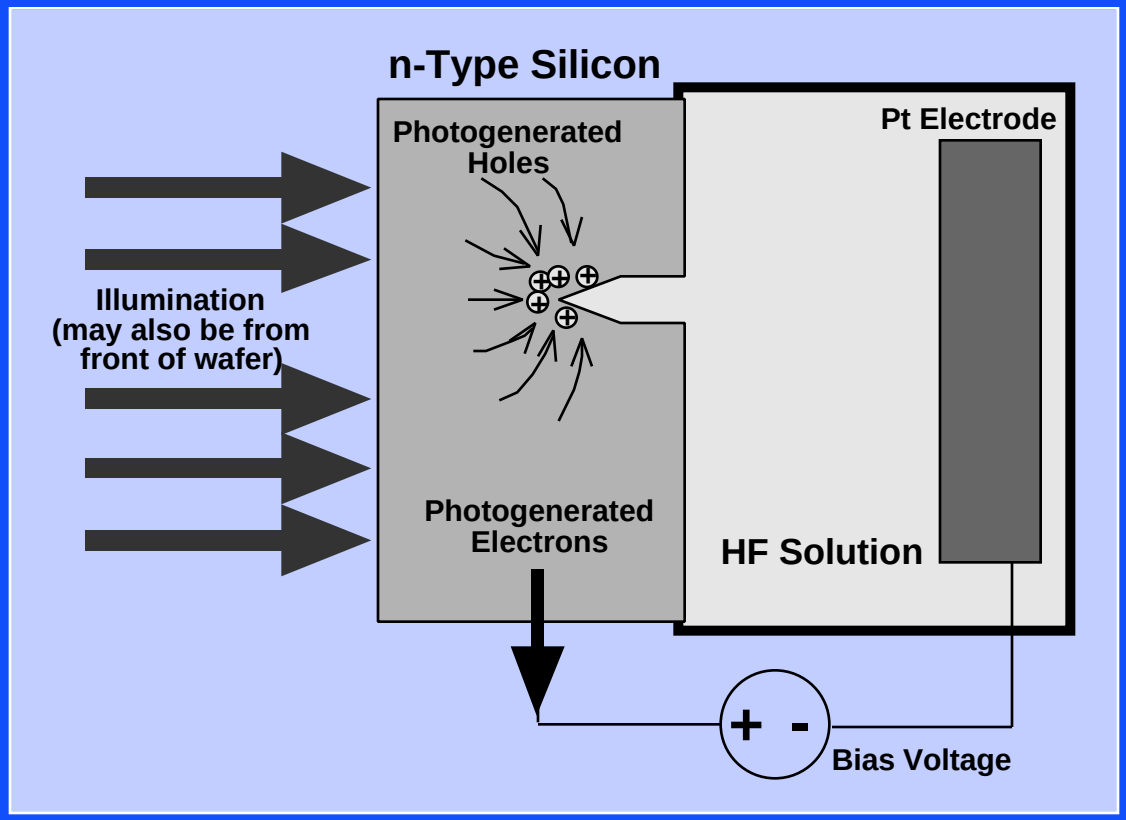




Courtesy Dr. Erno Klaassen, IBM Corp.

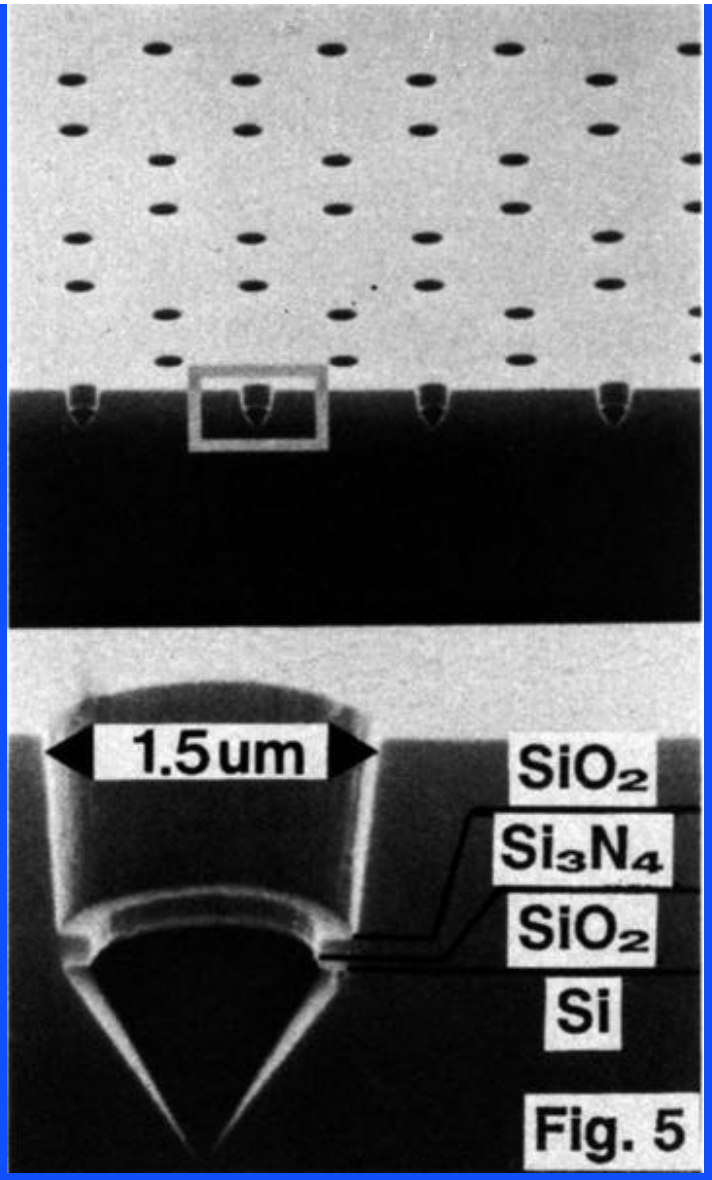
PHOTON-PUMPED ETCHING

- Use photogenerated electron-hole pairs to supply holes for etching reaction.
- Holes are concentrated at high-field points (deliberately started) and can yield holes with aspect ratios > 70:1.

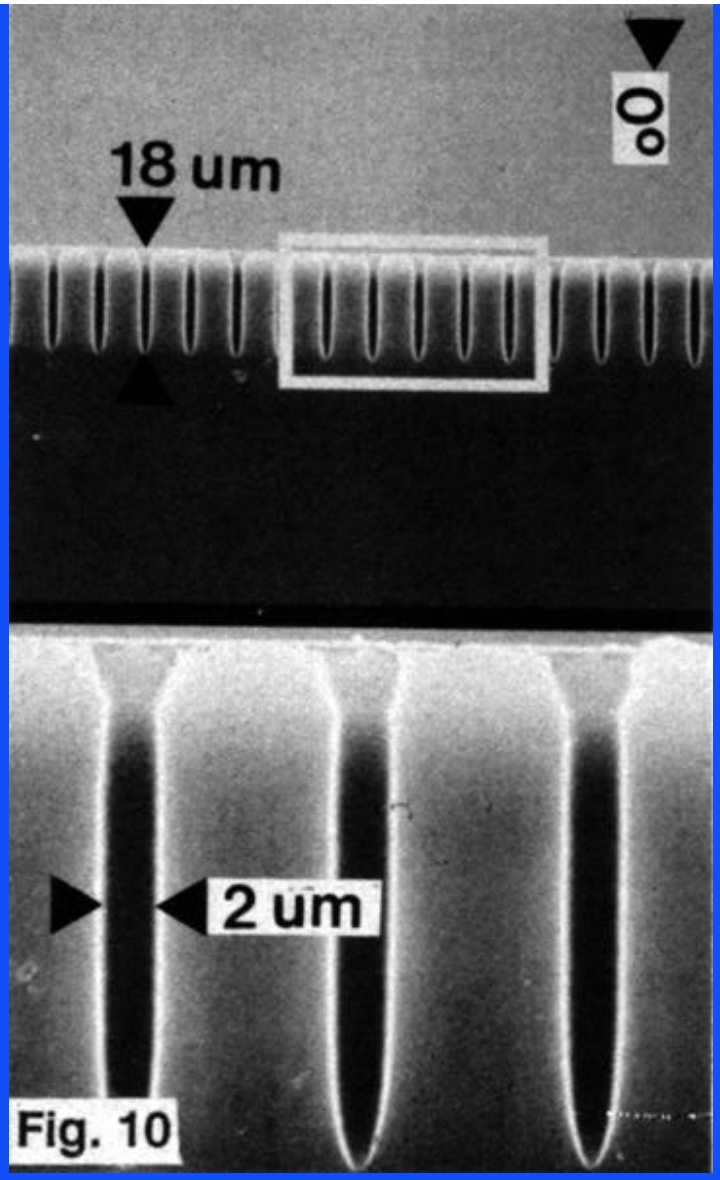


After Lehmann and Föll (1990).

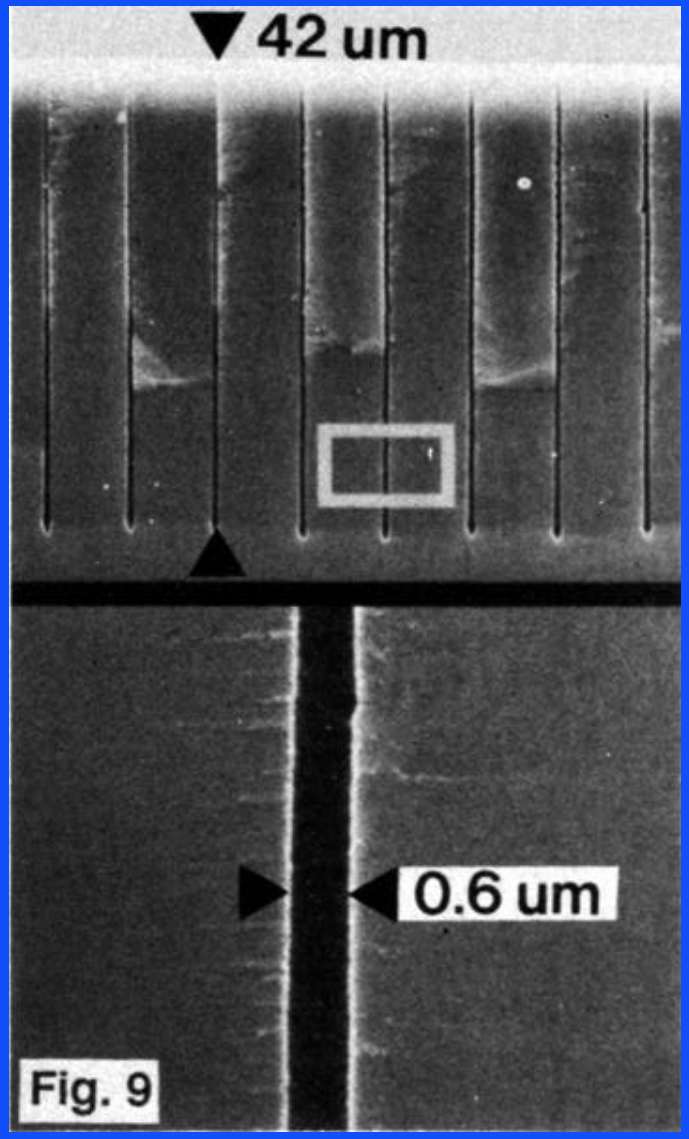
Lehmann, V., and Föll, H., "Formation Mechanism and Properties of Electrochemically Etched Trenches in n-Type Silicon," Journal of the Electrochemical Society, vol. 137, no. 2, Feb. 1990, pp. 653 - 659.



From Lehmann and Föll (1990).



Lehmann, V., and Föll, H., "Formation Mechanism and Properties of Electrochemically Etched Trenches in n-Type Silicon," Journal of the Electrochemical Society, vol. 137, no. 2, Feb. 1990, pp. 653 - 659.

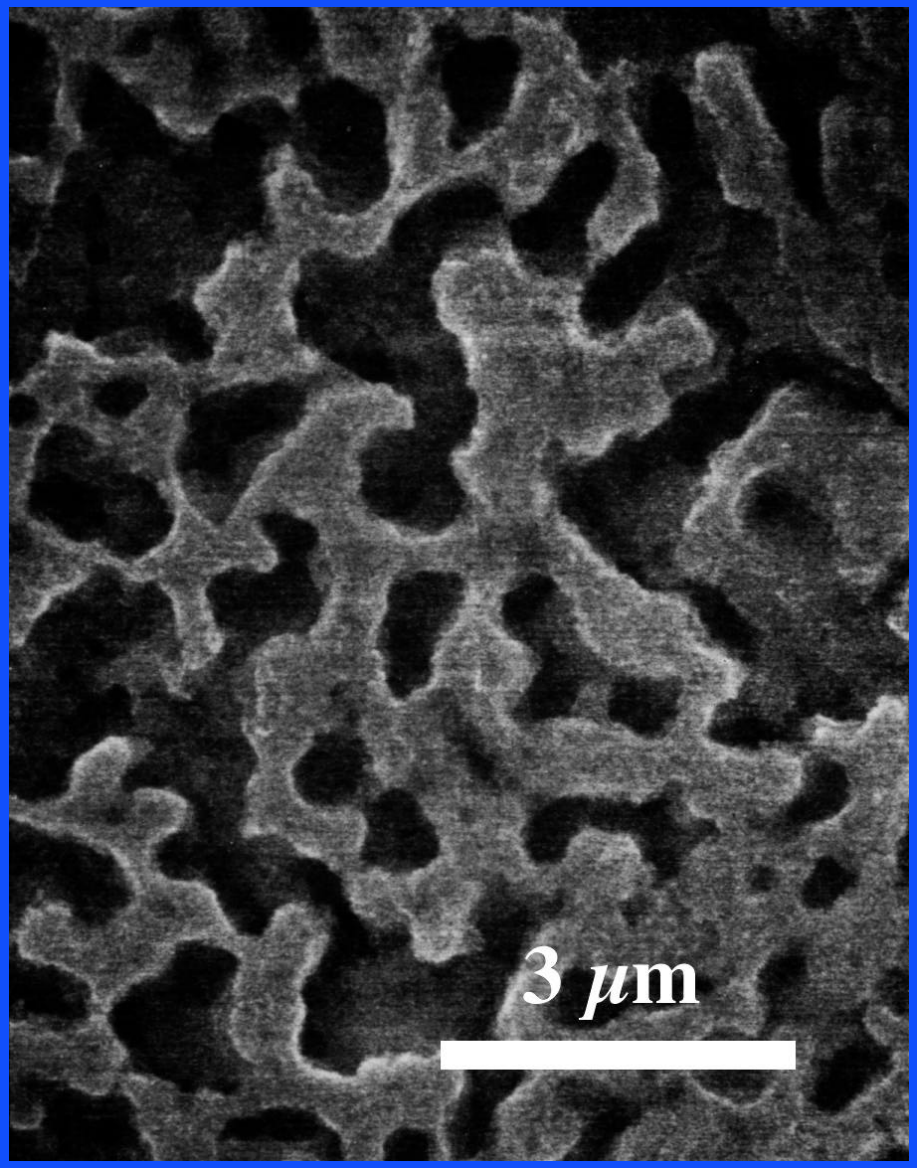


Lehmann, V., and Föll, H., "Formation Mechanism and Properties of Electrochemically Etched Trenches in n-Type Silicon," Journal of the Electrochemical Society, vol. 137, no. 2, Feb. 1990, pp. 653 - 659.

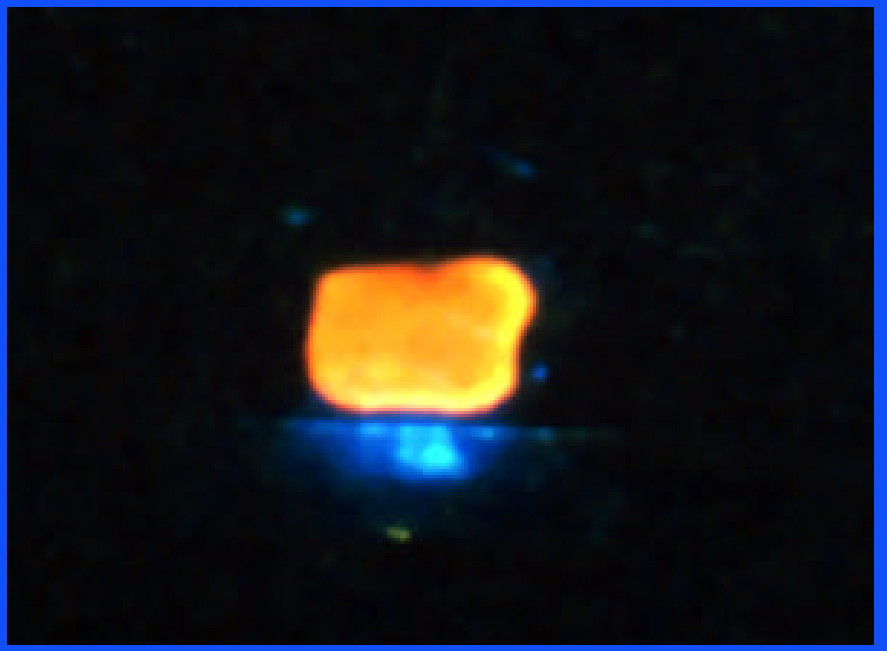
From Lehmann and Föll (1990).

POROUS SILICON

- If silicon etching is performed in very concentrated HF (i.e. 48% HF, 98 wt% ethanol) or solutions otherwise deficient in OH^-, with an anodic electrochemical bias on the silicon, the silicon is not fully oxidized during etching, producing a brownish film of porous silicon.
- The porous silicon is still single-crystal, but sponge-like since it is permeated by voids. Epitaxial Si can be grown over porous silicon.
- Porous silicon can have interesting optical properties, including fluorescence and electroluminescence (with an appropriate electrode).
- The density of the porous layer is controllable. The higher the applied current density during etching, the lower the density of the porous silicon (one can vary this over time to get buried lower density layers, for example). Silicon nitride works well as a mask.



Porous Silicon

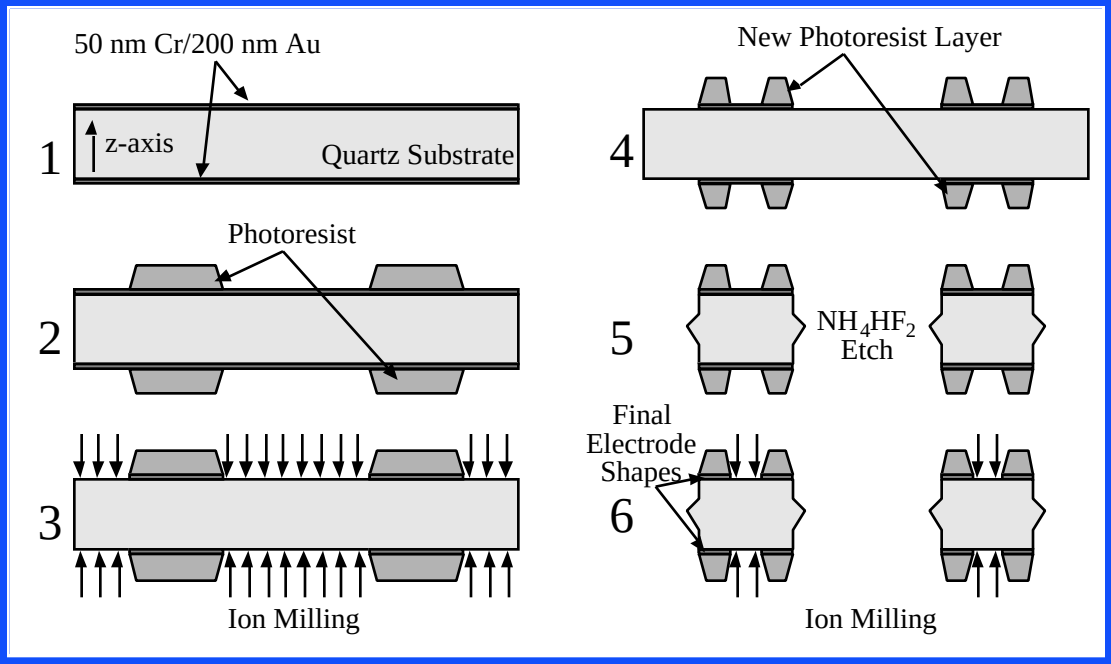


Porous silicon under UV illumination.

Images courtesy Prof. Nadim Maluf.

ANISOTROPIC ETCHING OF QUARTZ

Etchant Formula (mol/l)	x-Axis Etch Rate (μm/hr)	y-Axis Etch Rate (μm/hr)	z-Axis Etch Rate (μm/hr)
10.9 HF	0.02	< 0.005	9.6
7.2 HF + 4 NH_4F	0.025	0.005	2.55
5.4 NH_4NH_2	0.015	0.015	1.1
5.4 NH_4HF_2 + 1.8 NH_4F	0.015	0.015	0.75



After Toshiyoshi, et al. (1993).

Toshiyoshi, H., Fujita, H., Kawai, T., and Ueda, T., "Piezoelectrically Operated Actuators by Quartz Micromachining for Optical Applications," Proceedings of the IEEE Micro Electro Mechanical Systems Workshop, Fort Lauderdale, FL, Feb. 7 - 10, 1993, pp. 133 - 138.

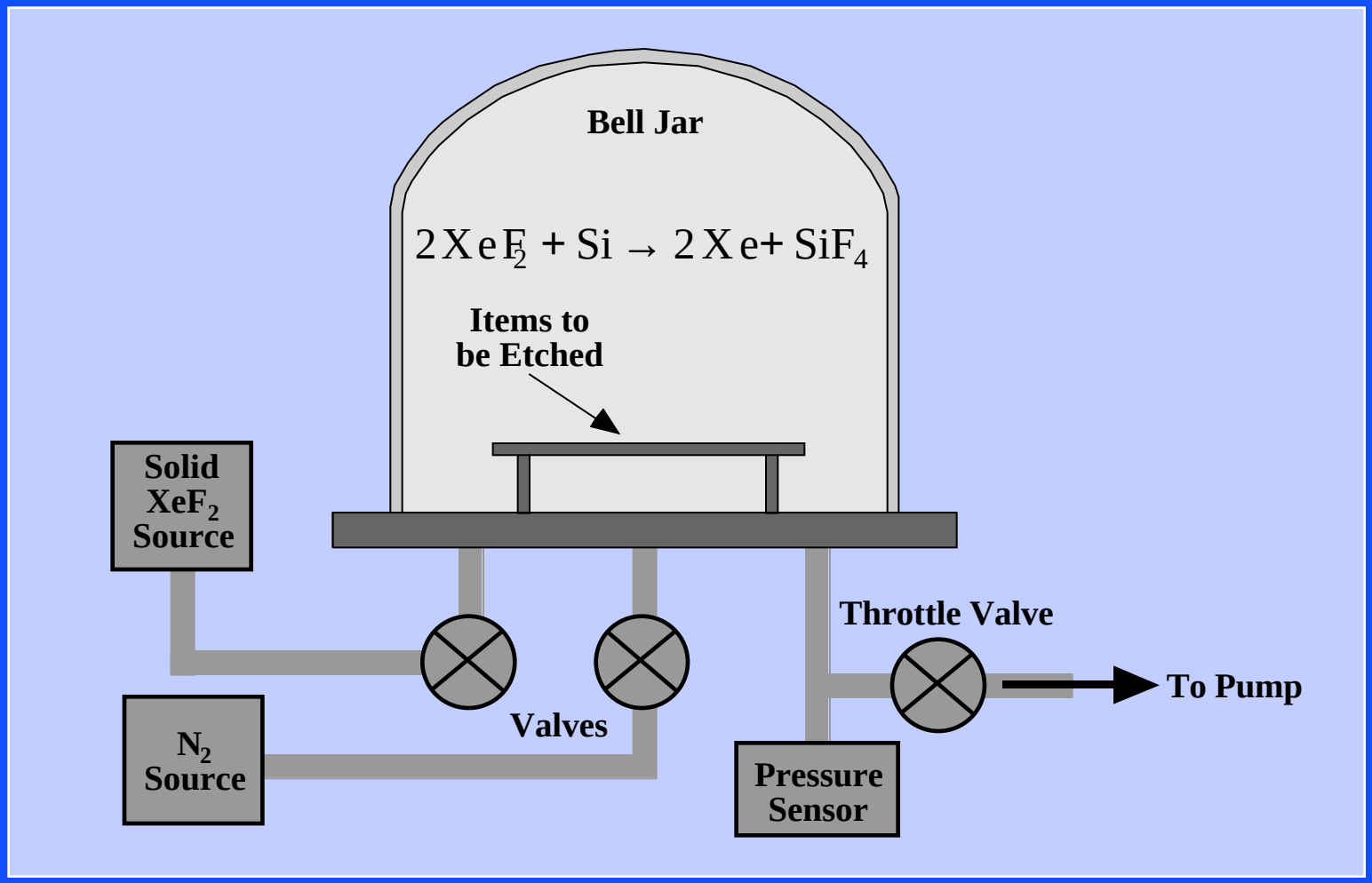
ETCHANT PROPERTIES (REMINDER)

- Selectivity to masking layer(s) and their availability.
- Selectivity to metals (e.g. Al).
- Etch rate.
- Anisotropy (crystal plane selectivity).
- Surface roughness.
- Control of etch parameters.
- Safety of reactant(s) and product(s).
- Cost (including disposal and fixed costs).
- Capacity for etch-stops.
- Mode and ease of use (including throughput).
- Other parameters?

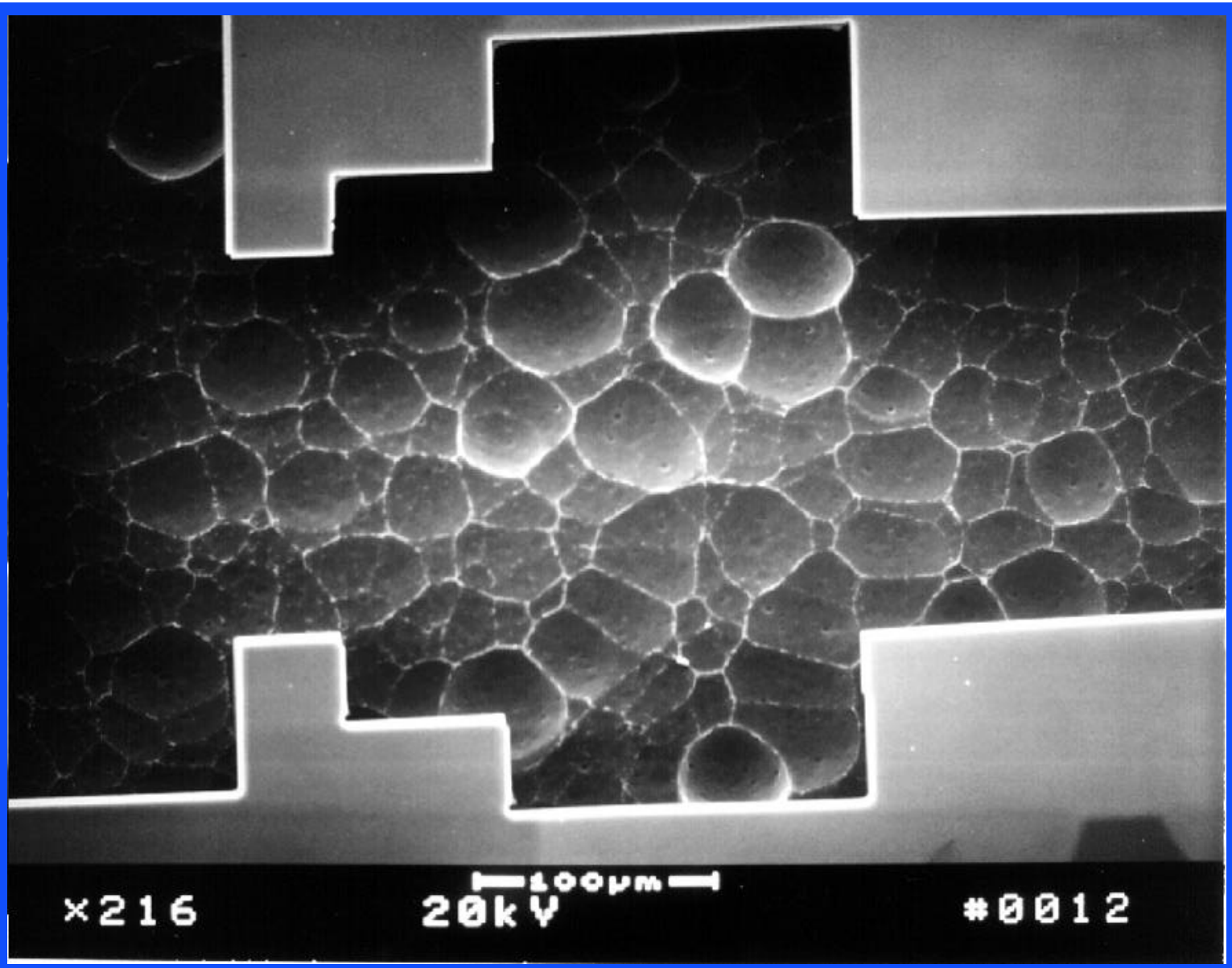
DRY SILICON ETCHING

- XeF_2 vapor etching provides simple, isotropic silicon etching with no appreciable attack of aluminum, silicon dioxide, silicon nitride, etc. (alternates are the interhalogens, such as BrF_3).
- Plasma etching uses the generation of reactive ions and free radical species (such as monoatomic fluorine) by electron bombardment at low pressure.
- Silicon and other materials can be etched by forming volatile compounds.
- Reactive Ion Enhanced (RIE) Etching allows for higher energy ions and can yield much greater anisotriopy.
- Advanced RIE techniques can yield extremely vertical walls.

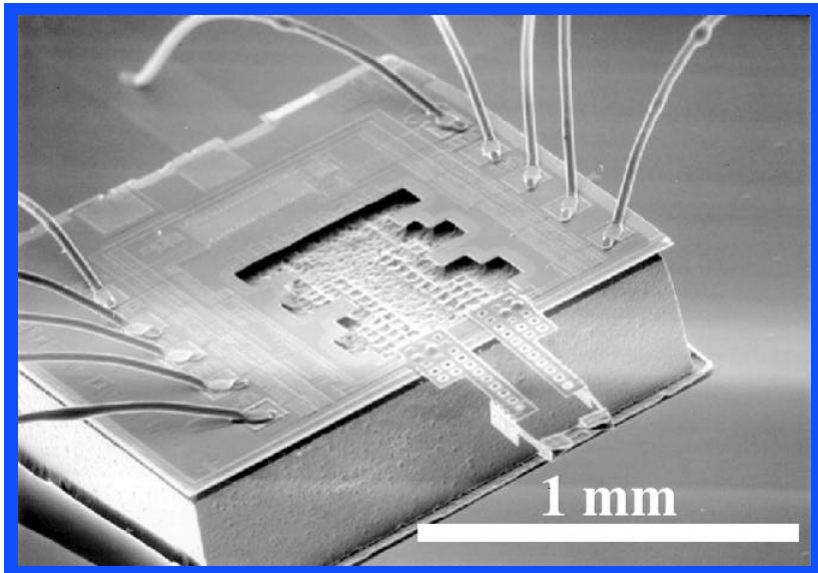
XeF_2 ETCHING SYSTEM

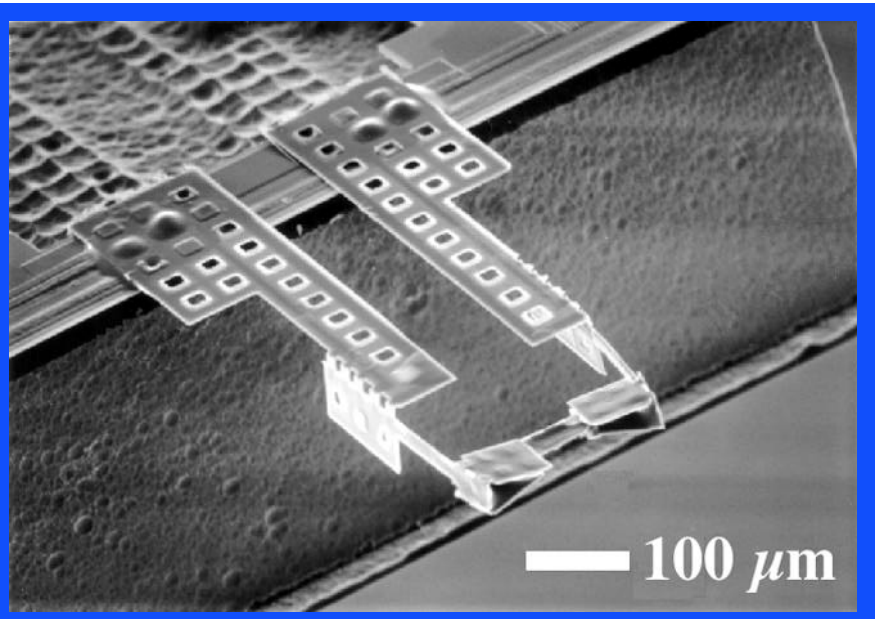


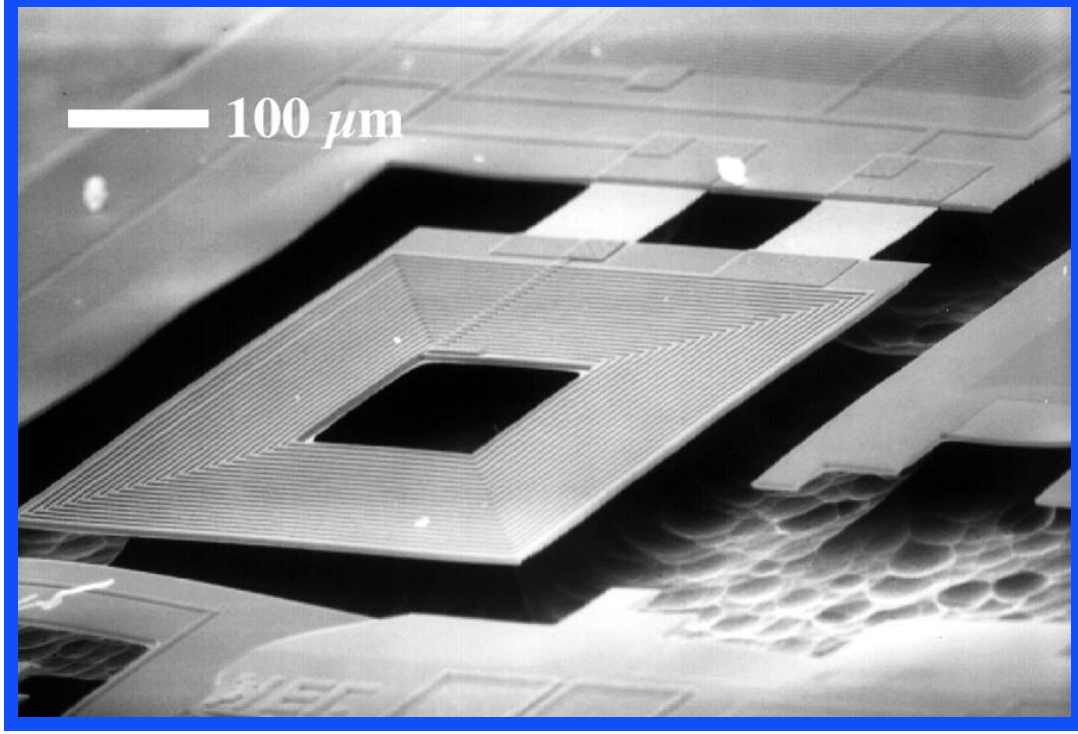
After Hoffman, et al., (1995).



Courtesy Prof. K. Pister, U.C. Berkeley.

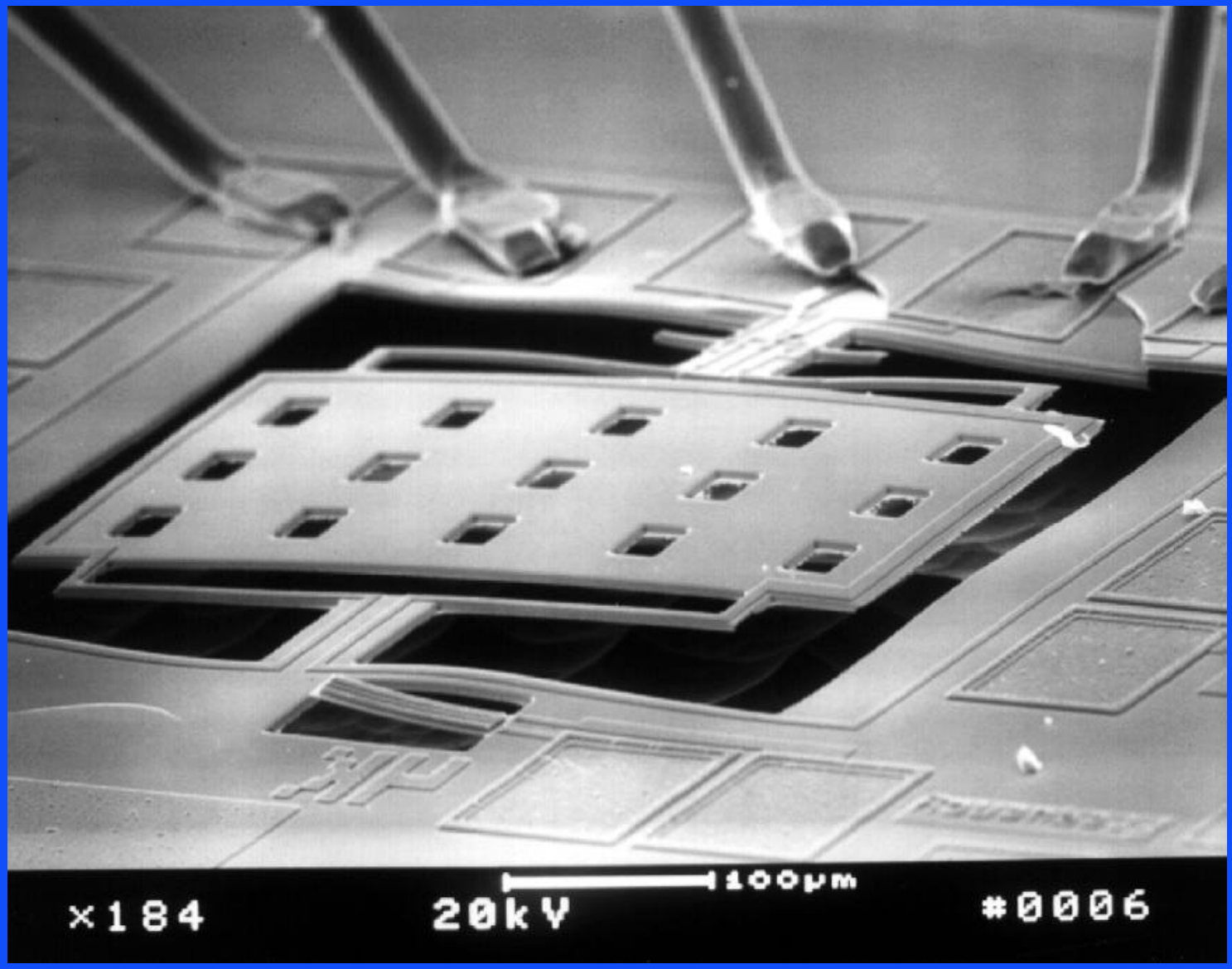






Courtesy Prof. K. Pister, U.C. Berkeley.

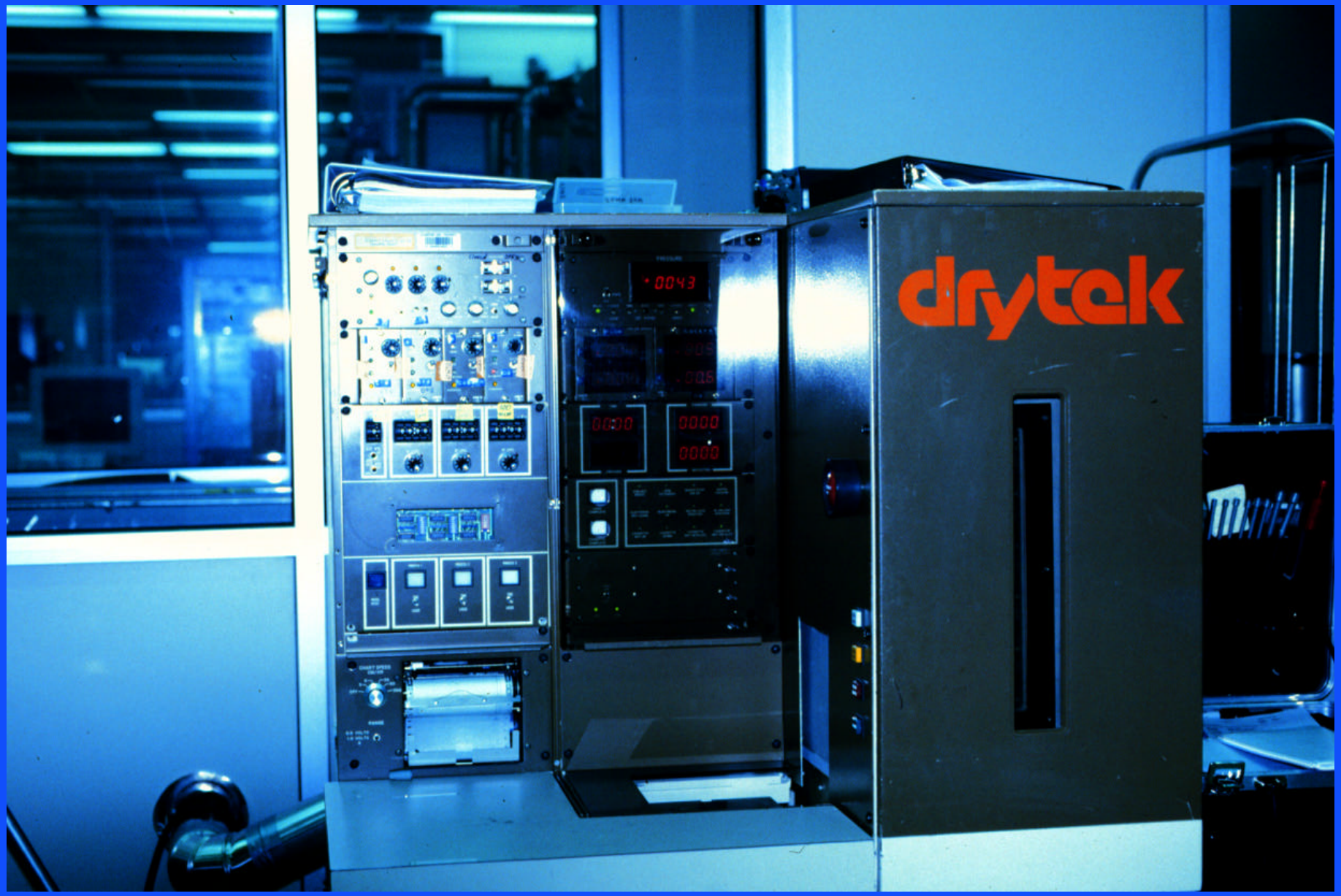
Reference: Hoffman, E., Warneke, B., Kruglick, E., Weigold, J., and Pister, K. S. J., "3D Structures with Piezoresistive Sensors in Standard CMOS," Proceedings of the IEEE Micro Electro Mechanical Systems Conference, Amsterdam, Netherlands, Jan. 29 - Feb. 2, 1995, pp. 288 - 293.

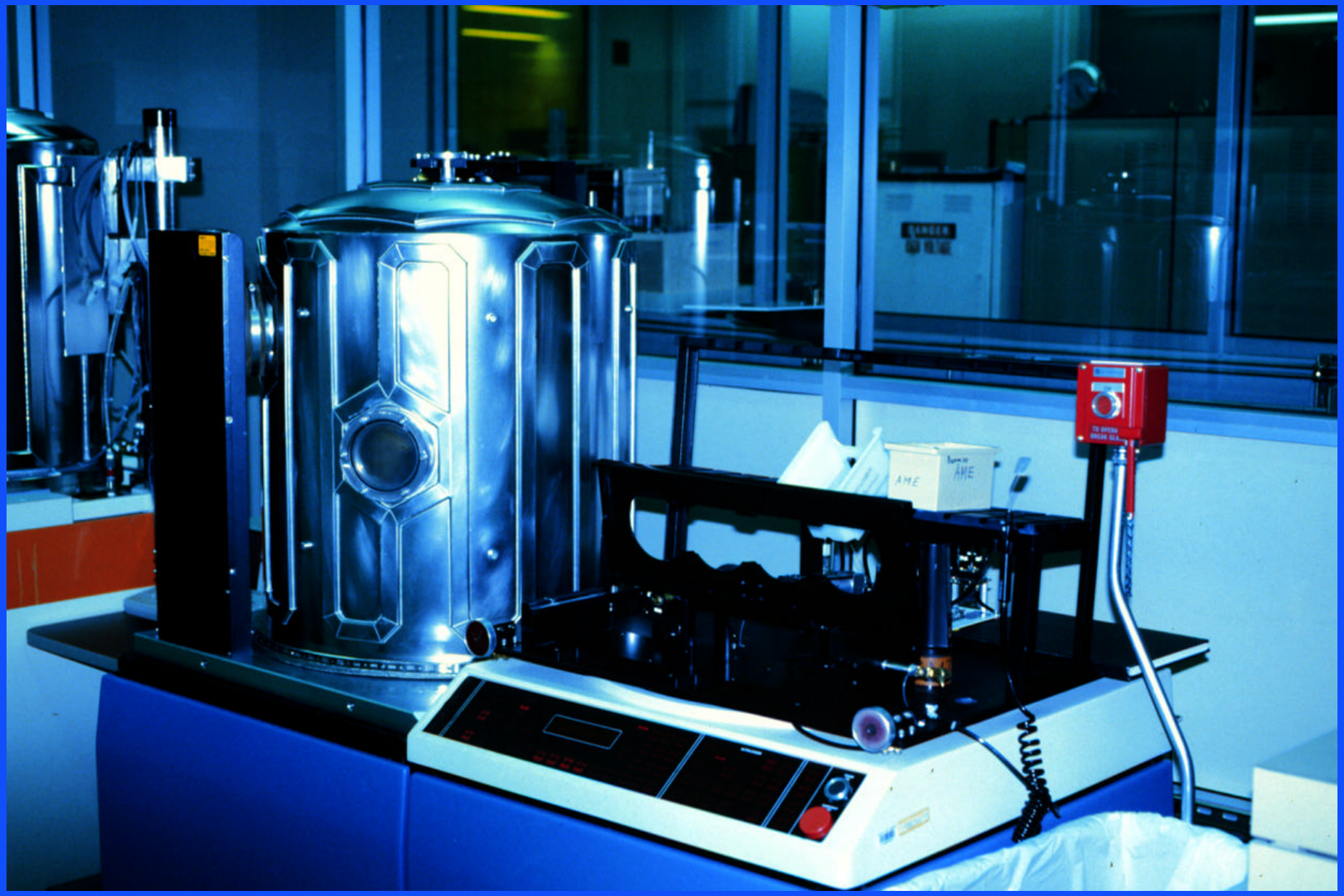


Courtesy Prof. K. Pister, U.C. Berkeley.

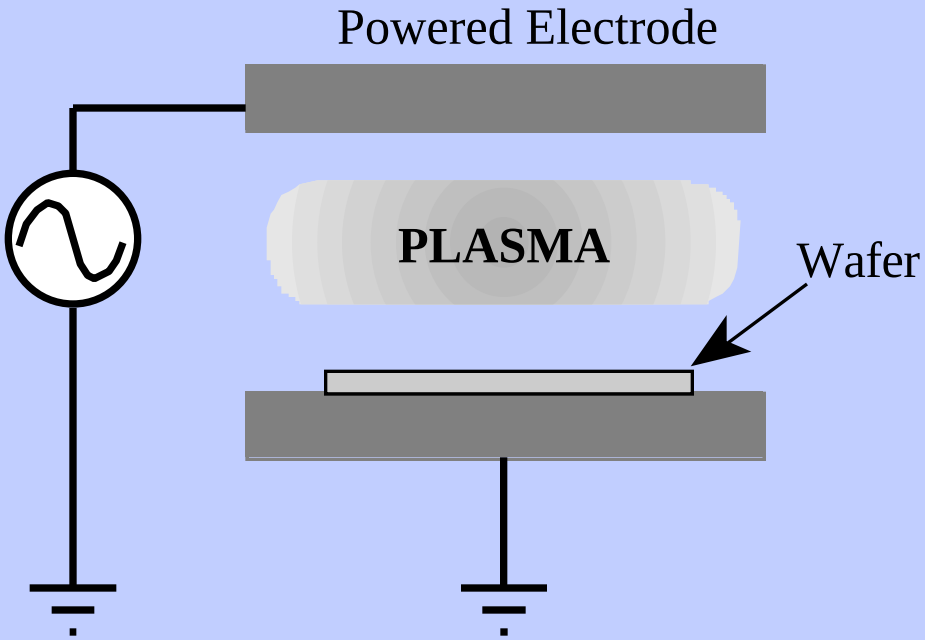
PLASMA/RIE ETCHING

- **Plasma/RIE etching uses RF energy to drive reactions, taking the place of elevated temperatures or inherently reactive starting chemicals.**
- **RF energy is applied to plates, causing stray electrons to be accelerated.**
- **The electrons hit reactant molecules, forming reactive ions and radicals.**
- **Glow region is roughly charge-neutral.**
- **Dark “sheath” regions near electrodes are high field to retard transit of electrons which are more mobile... this sheath bias can accelerate ions.**

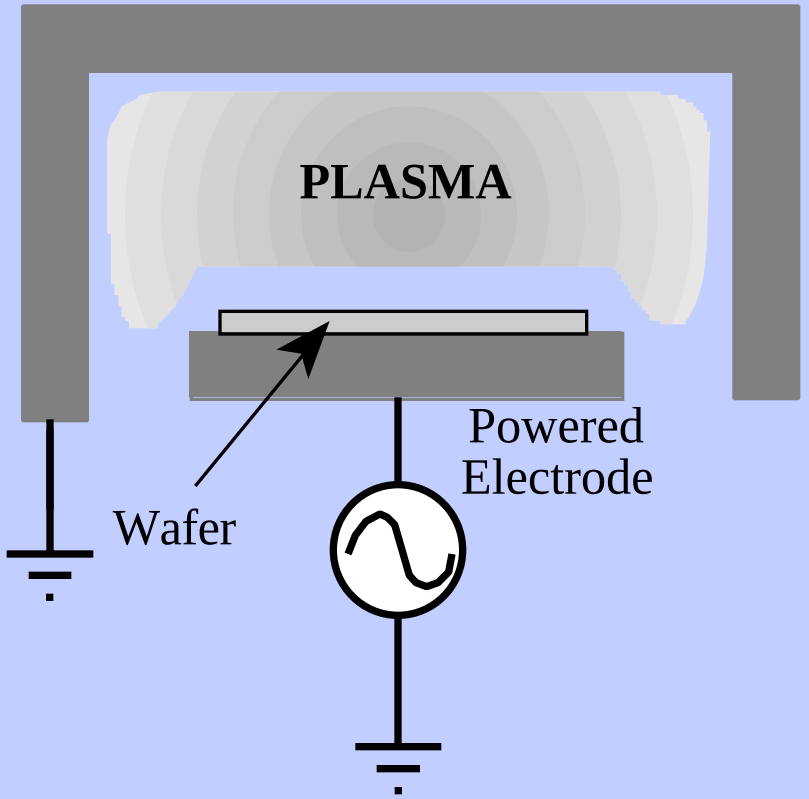




PLASMA ETCHER



REACTIVE ION ETCHER



EXAMPLE PLASMA CHEMISTRY

Dissociation Reactions

$e^- + SF_6 \rightarrow SF_5 + F + e^-$

$e^- + SF_5 \rightarrow SF_4 + F + e^-$

$e^- + SF_4 \rightarrow SF_3 + F + e^-$

Ionization Reactions

$e^- + SF_6 \rightarrow SF_5^+ + F + 2e^-$

$e^- + SF_6 \rightarrow SF_3^+ + F_2 + F + 2e^-$

$e^- + SF_4 \rightarrow SF_3^+ + F + 2e^-$

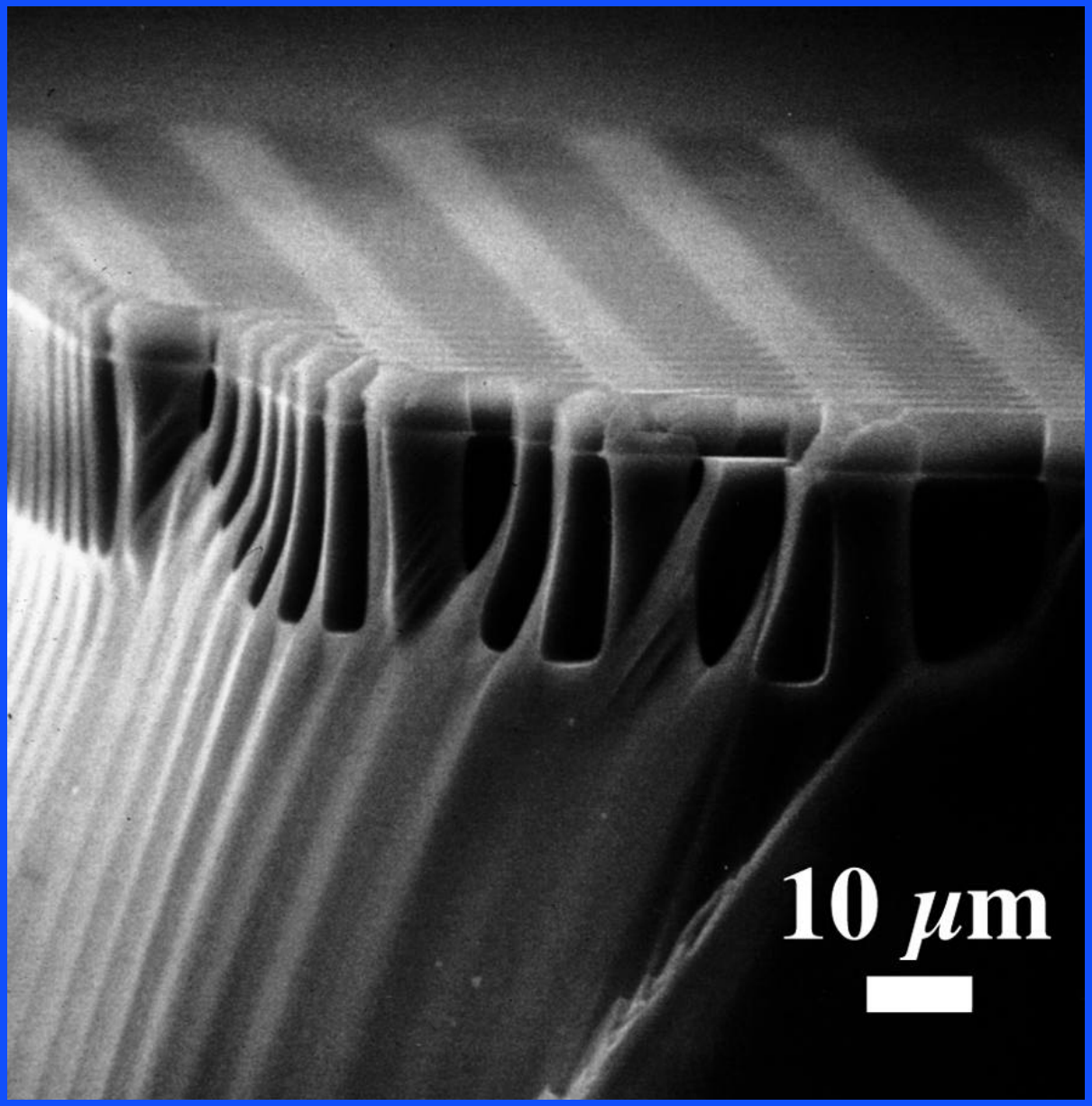
Attachment Reactions

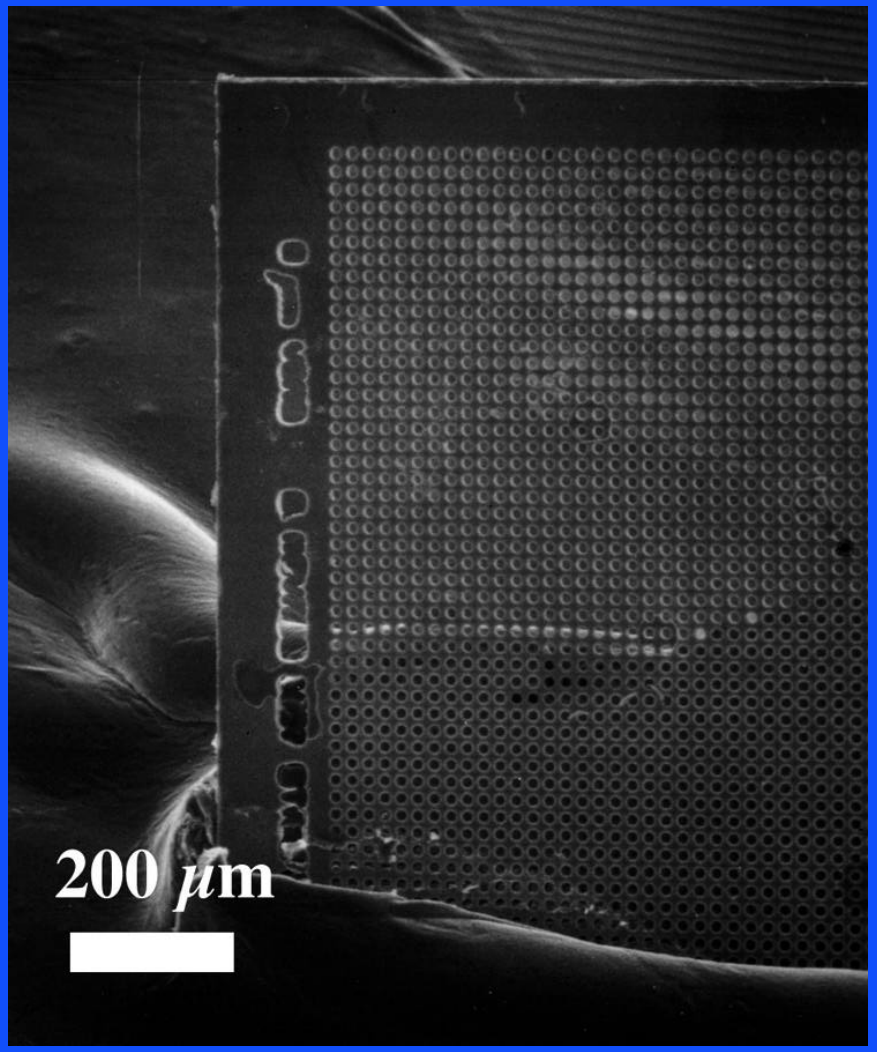
$e^- + SF_6 \rightarrow SF_5^- + F$

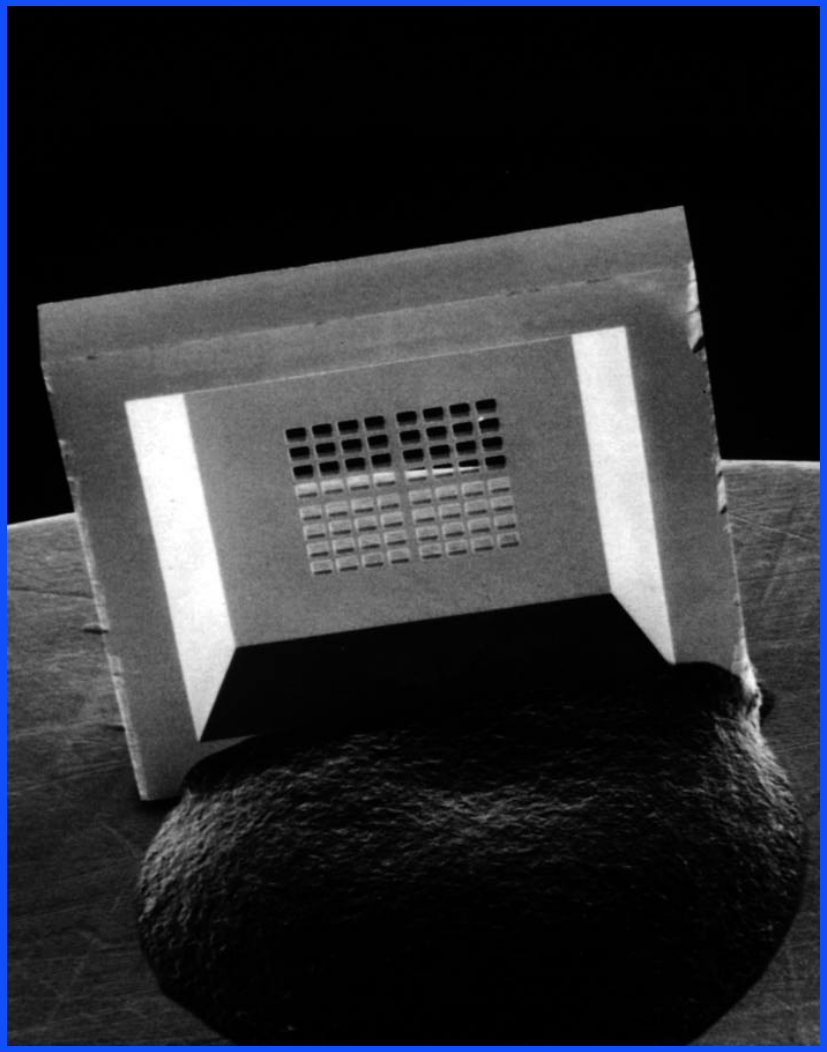
$e^- + SF_4 \rightarrow SF_3^- + F$

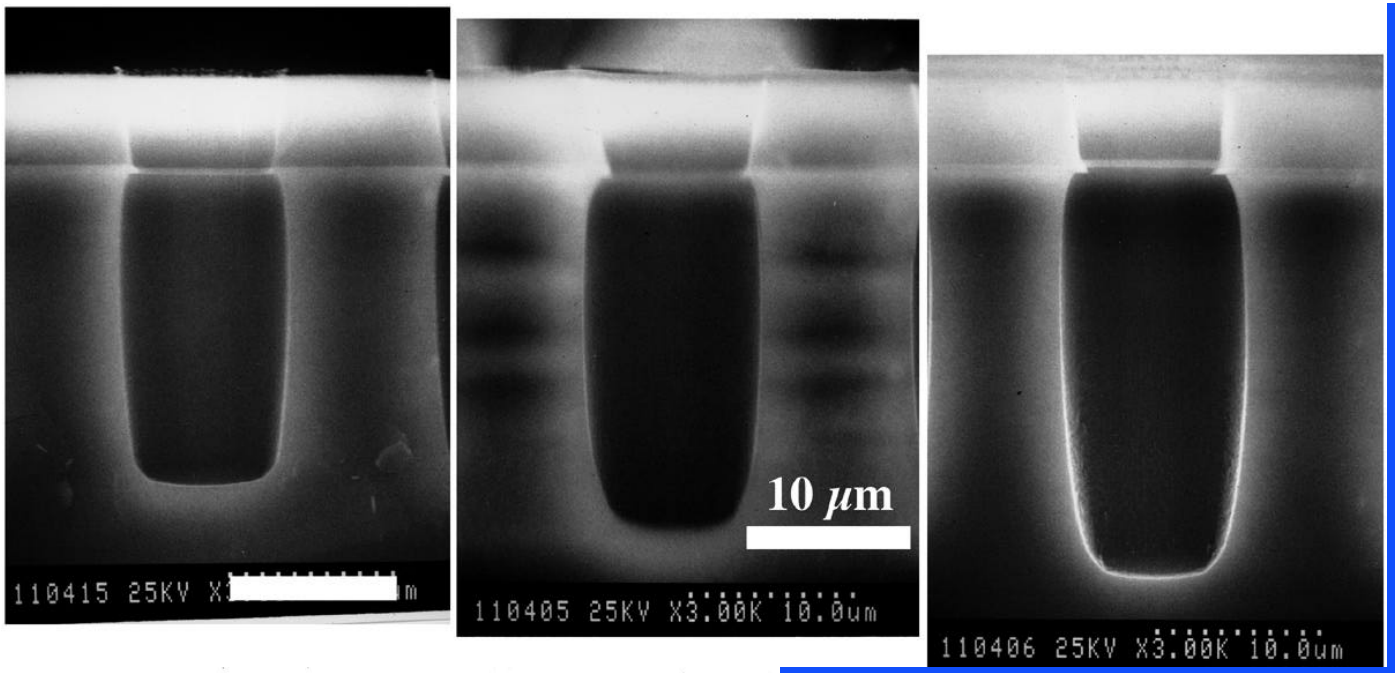
$e^- + SF_4 \rightarrow SF_3^+ + F + 2e^-$

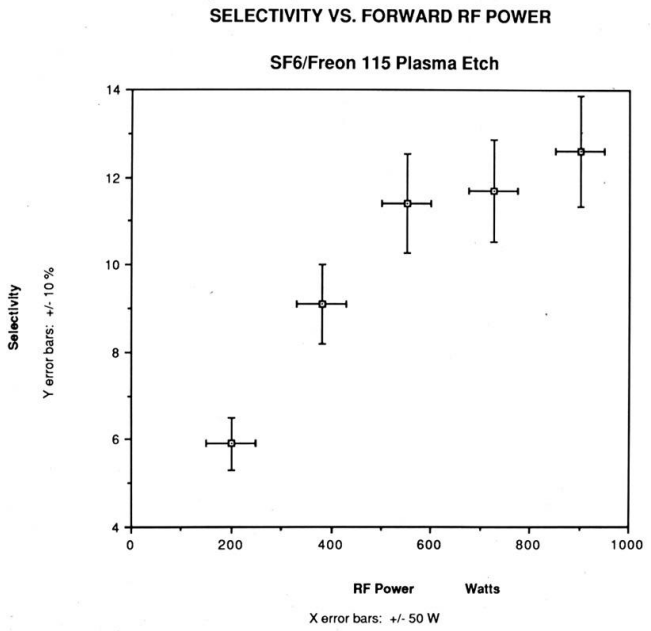
$SiF_x + F \rightarrow SiF_{x+1}$ where x = 0 to 3



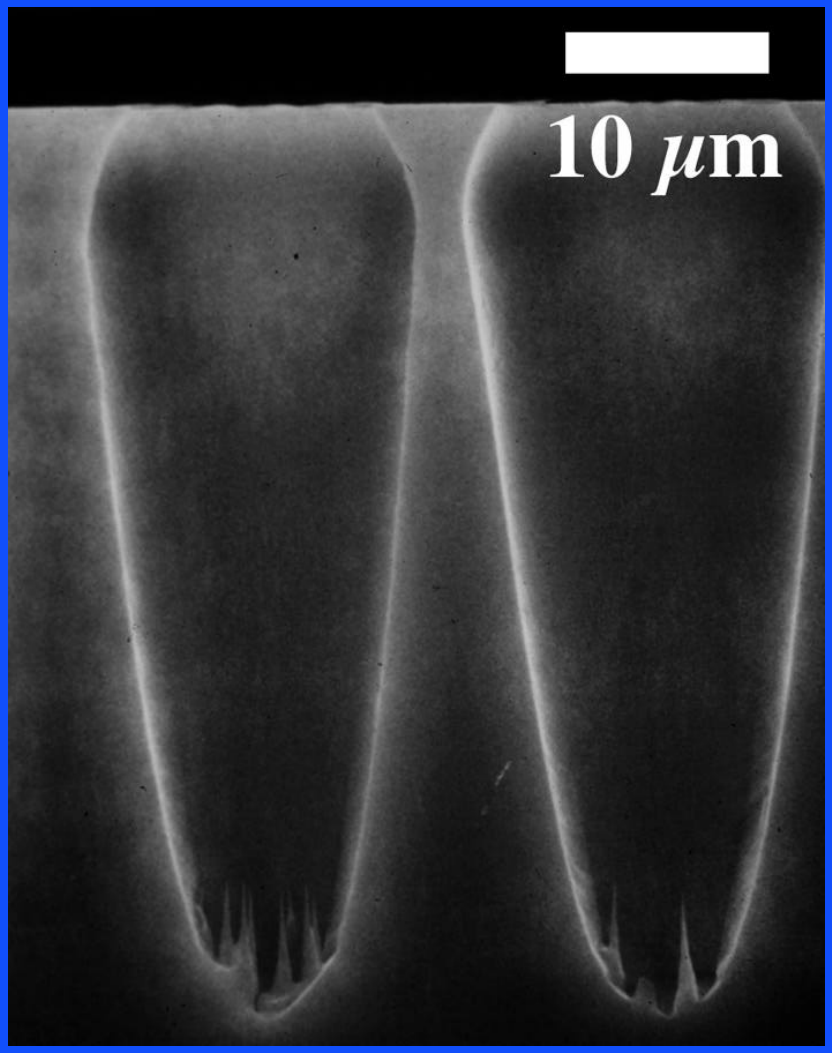


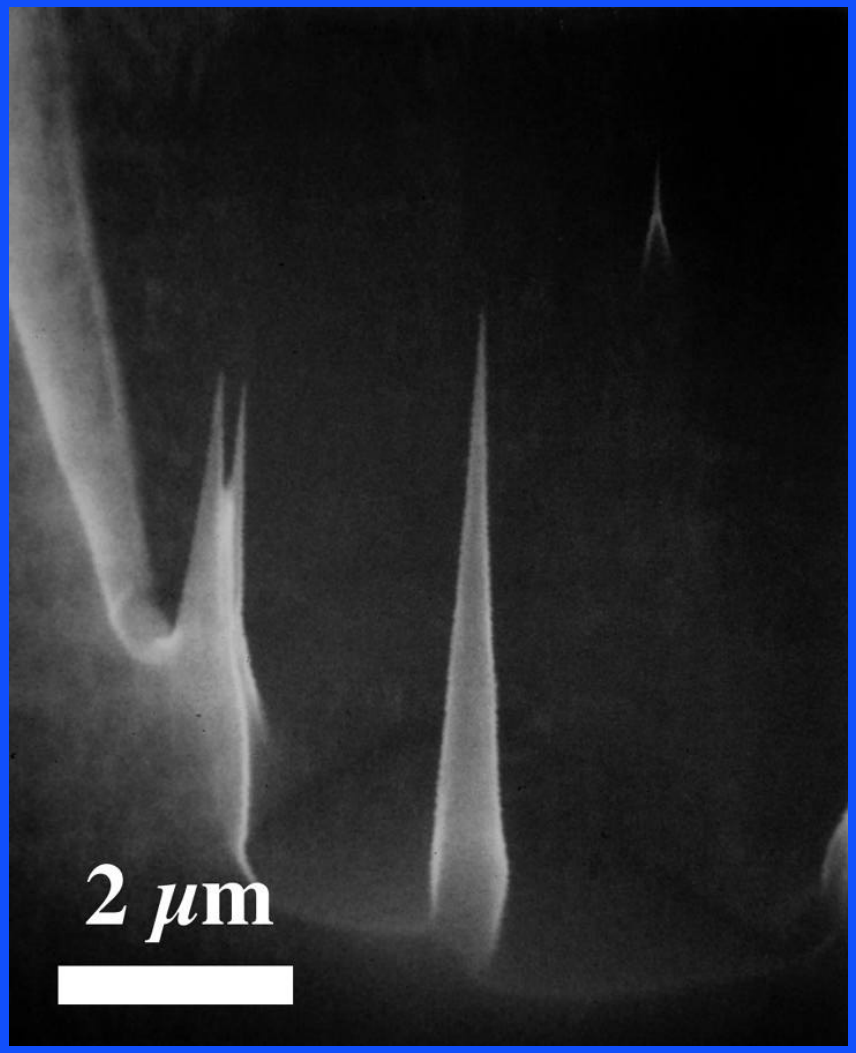


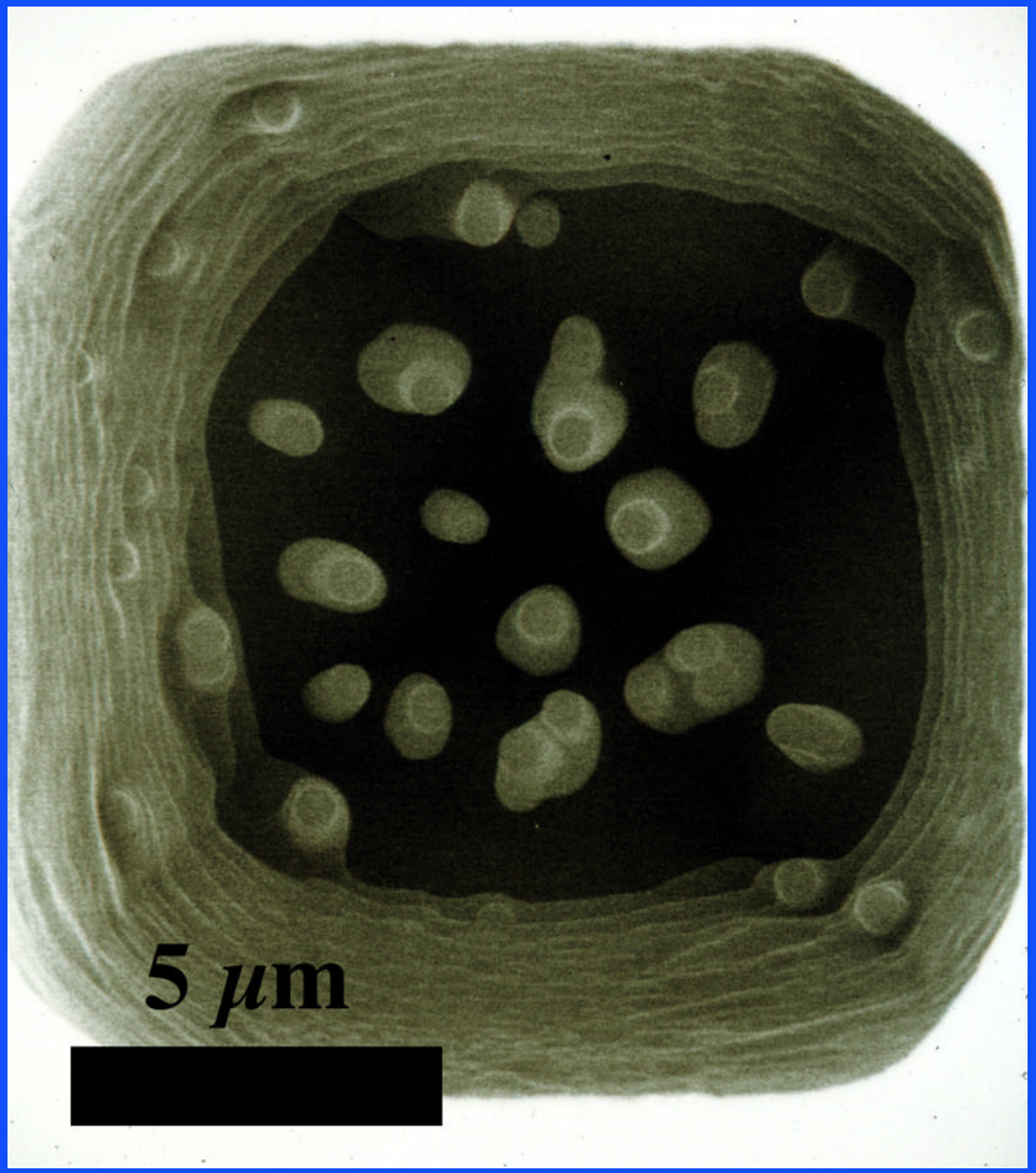


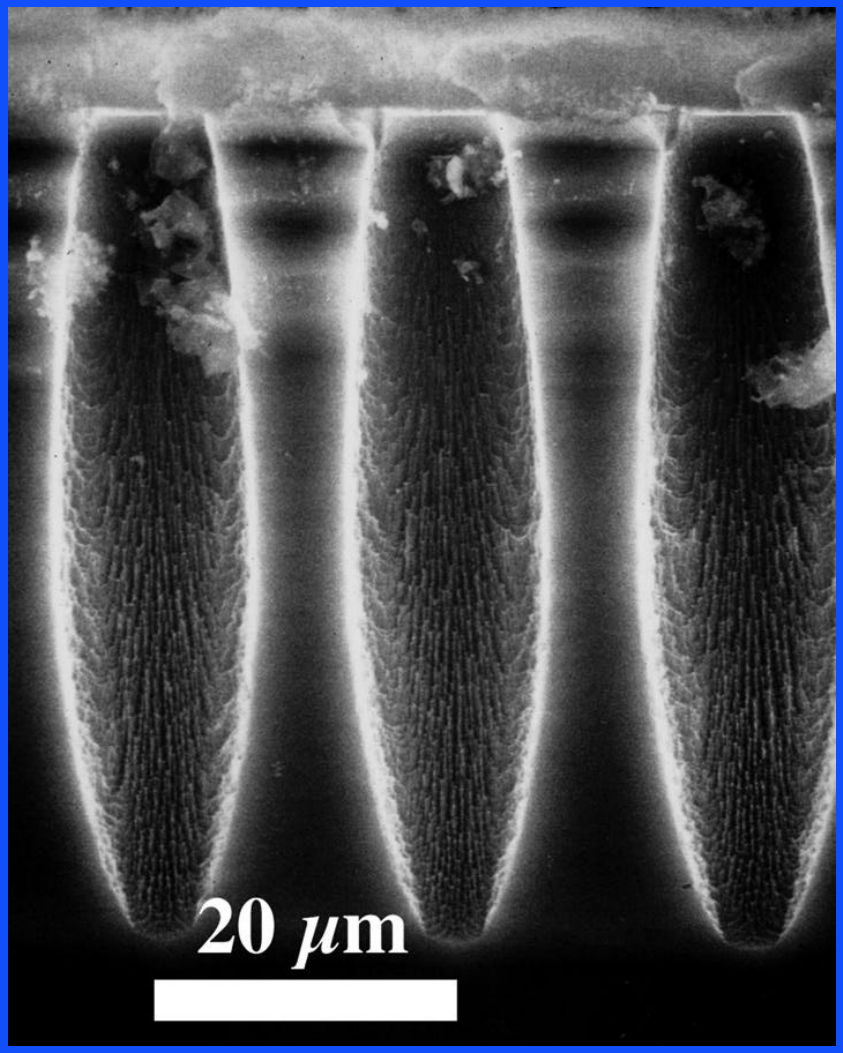


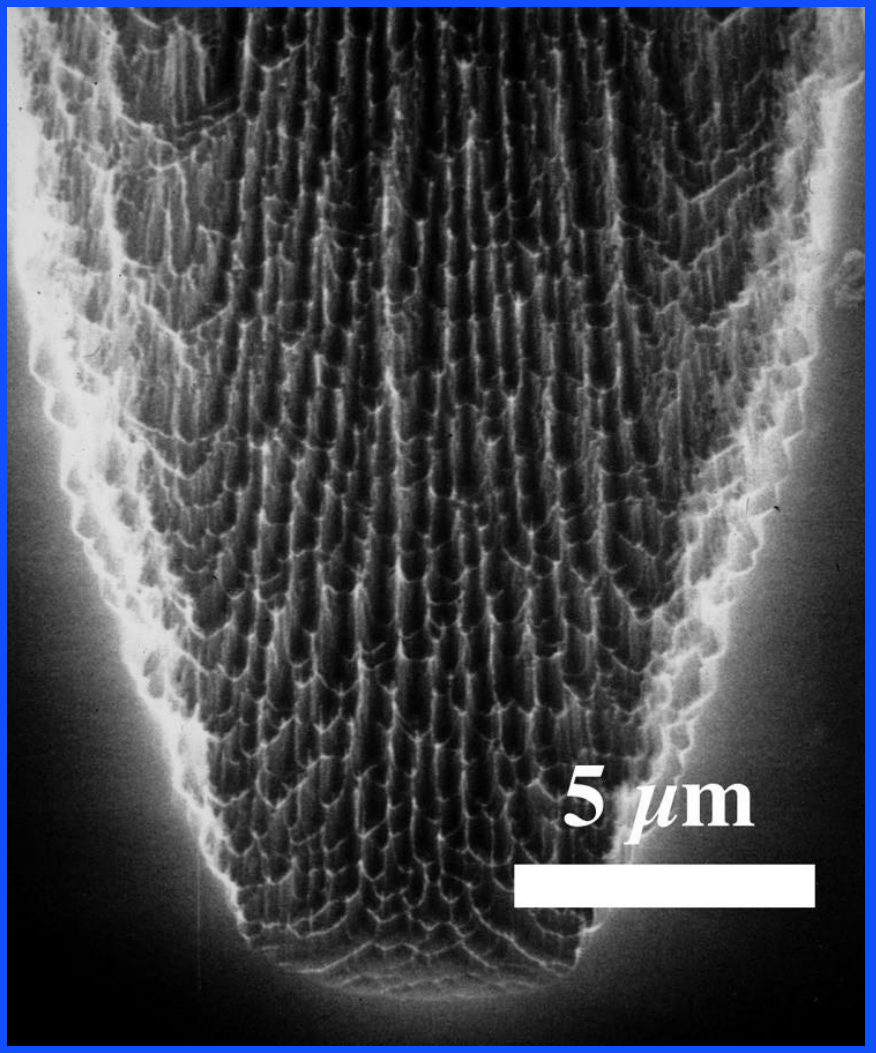
- Example plasma etch series showing change in shape and photoresist selectivity versus applied RF power.
- There are always many variables in plasma etching, some in the control of the user and some not.

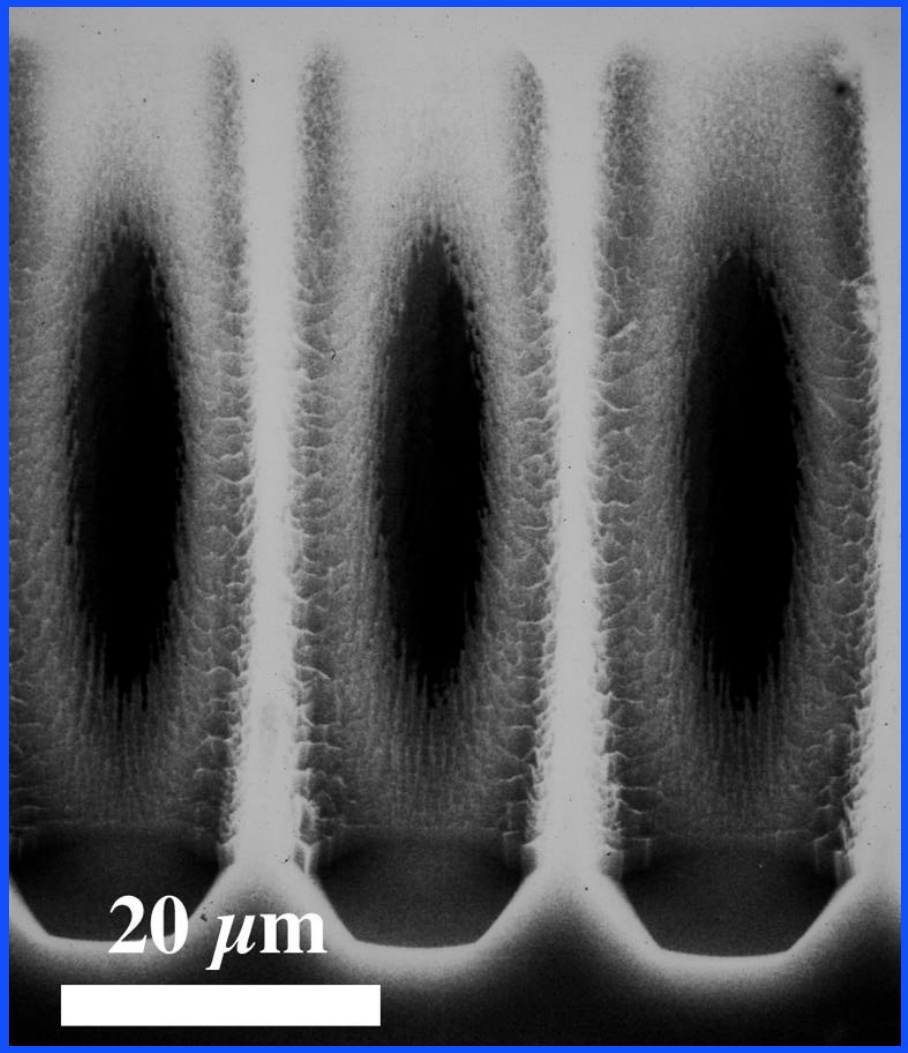


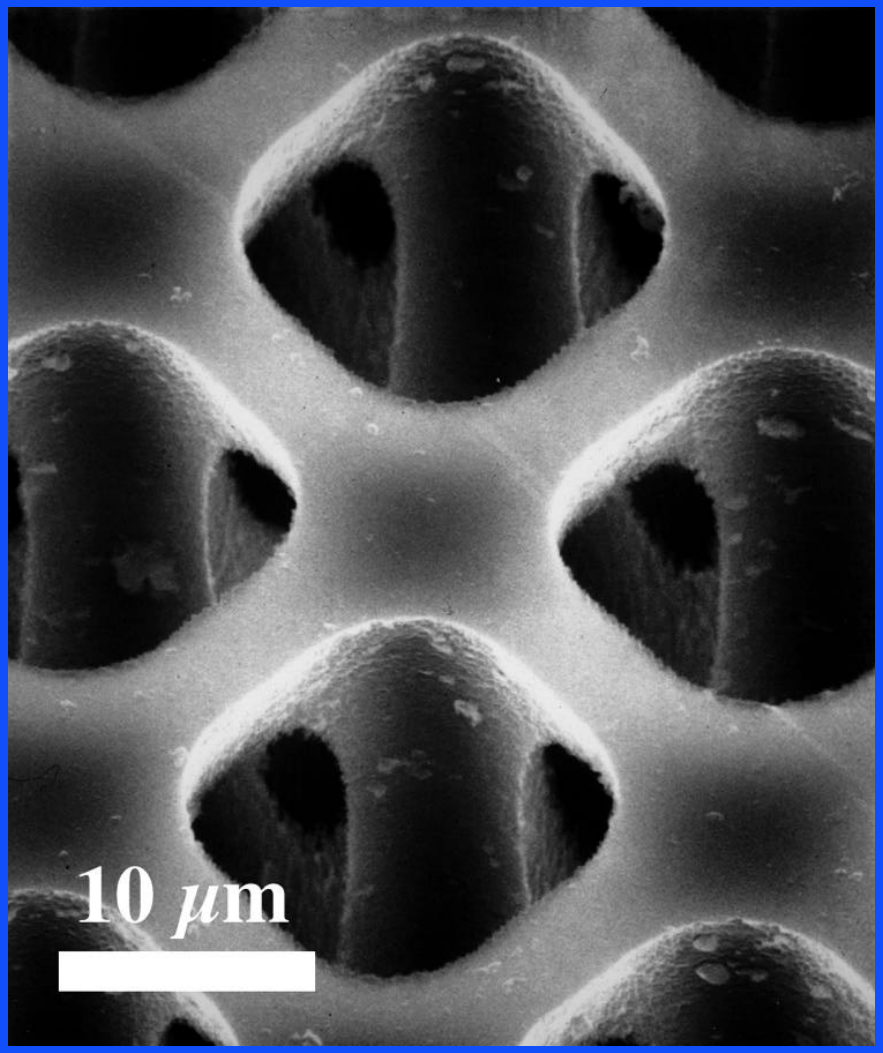


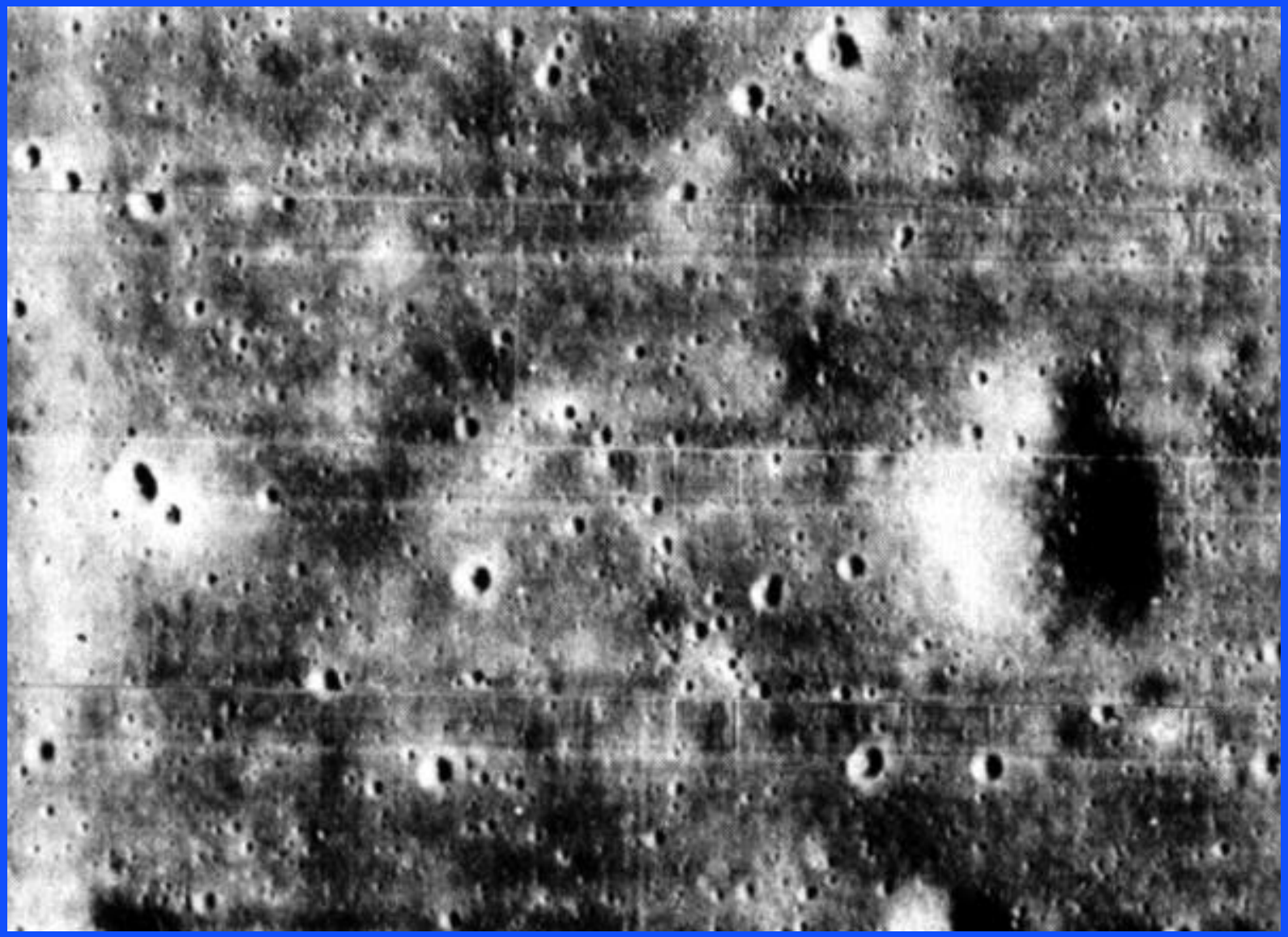


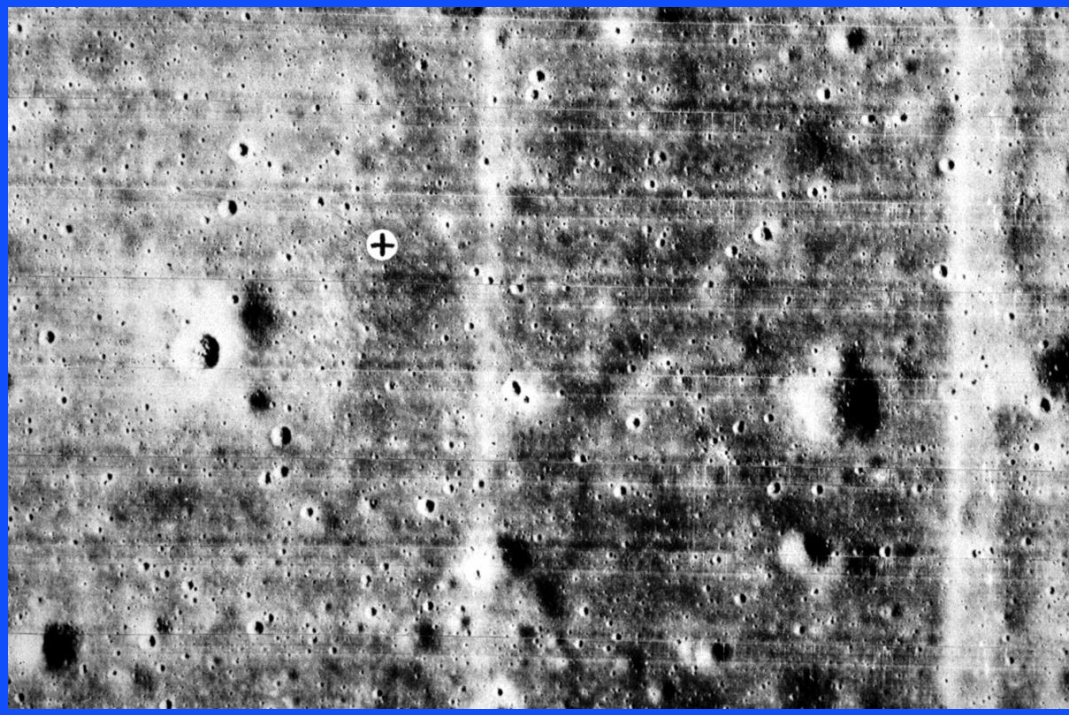






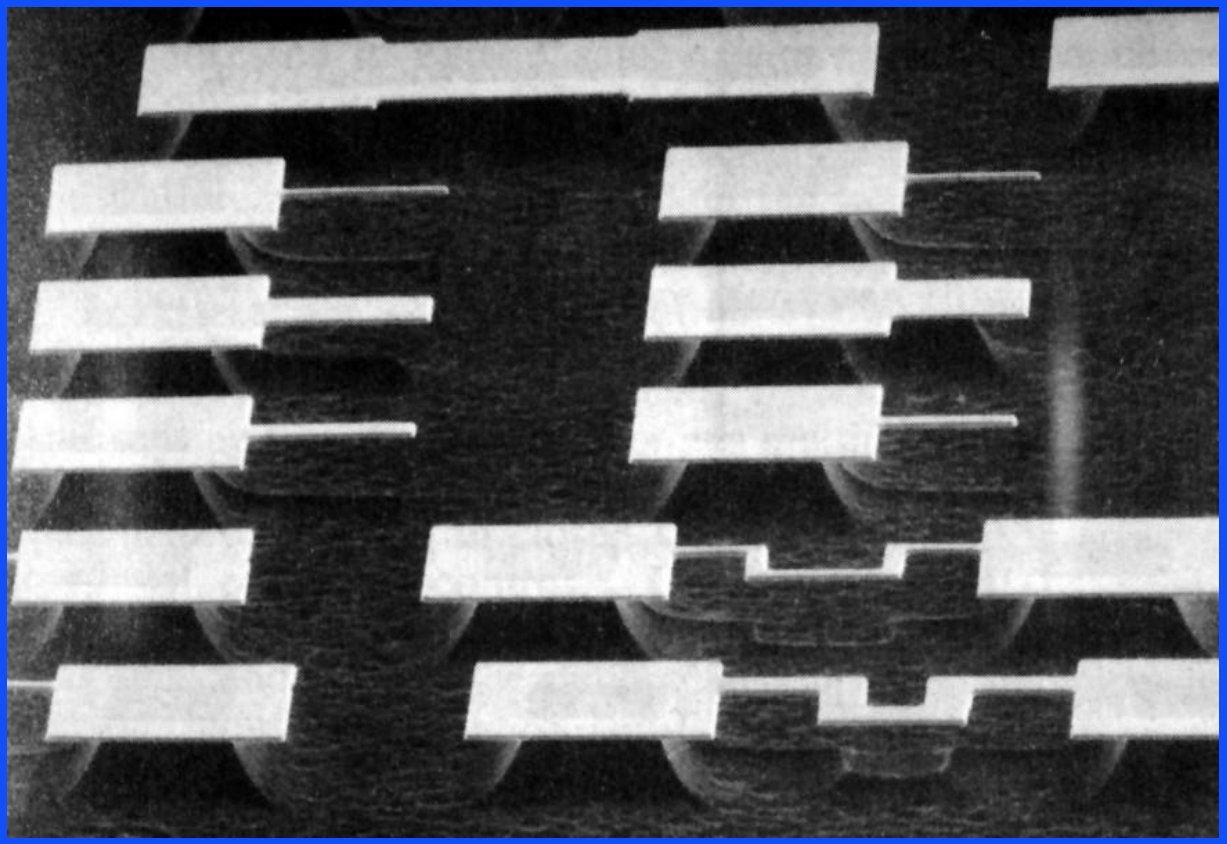






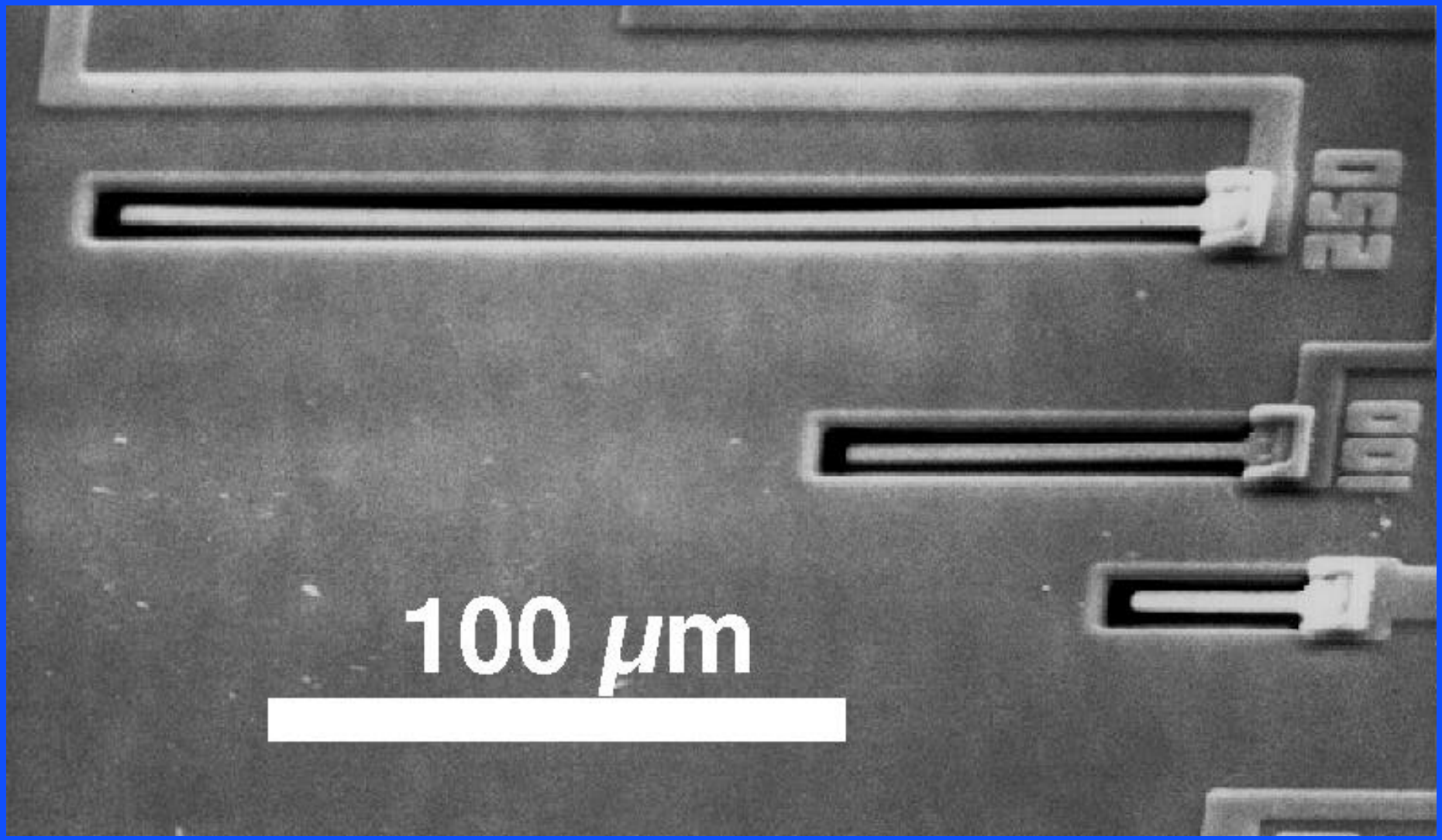
Source: NASA

PLASMA UNDERCUT STRUCTURES



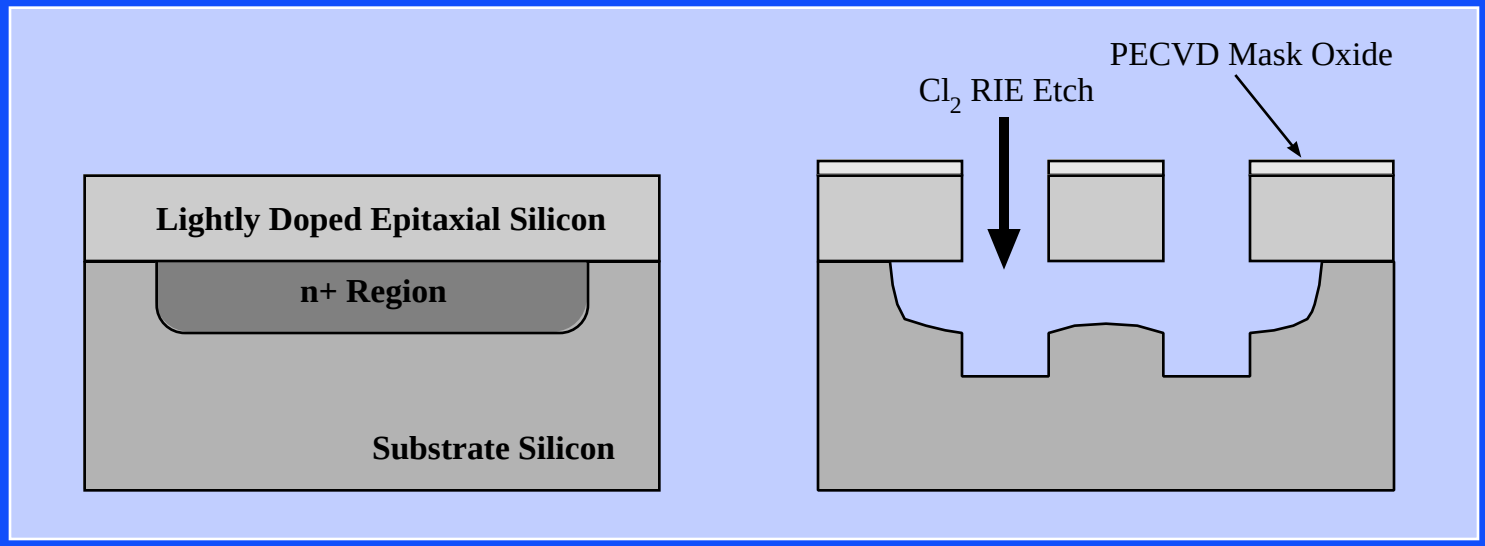
Source: Linder, C., Tschan, T., and de Rooij, N. F., "Deep Dry Etching Techniques as a New IC Compatible Tool for Silicon Micromachining," Proceedings of Transducers '91, the 1991 International Conference on Solid-State Sensors and Actuators Digest of Technical Papers, IEEE Press, San Francisco, CA, June 24 - 27, 1991, pp. 524 - 527.

UNDERCUTTING Al ON STANDARD CMOS



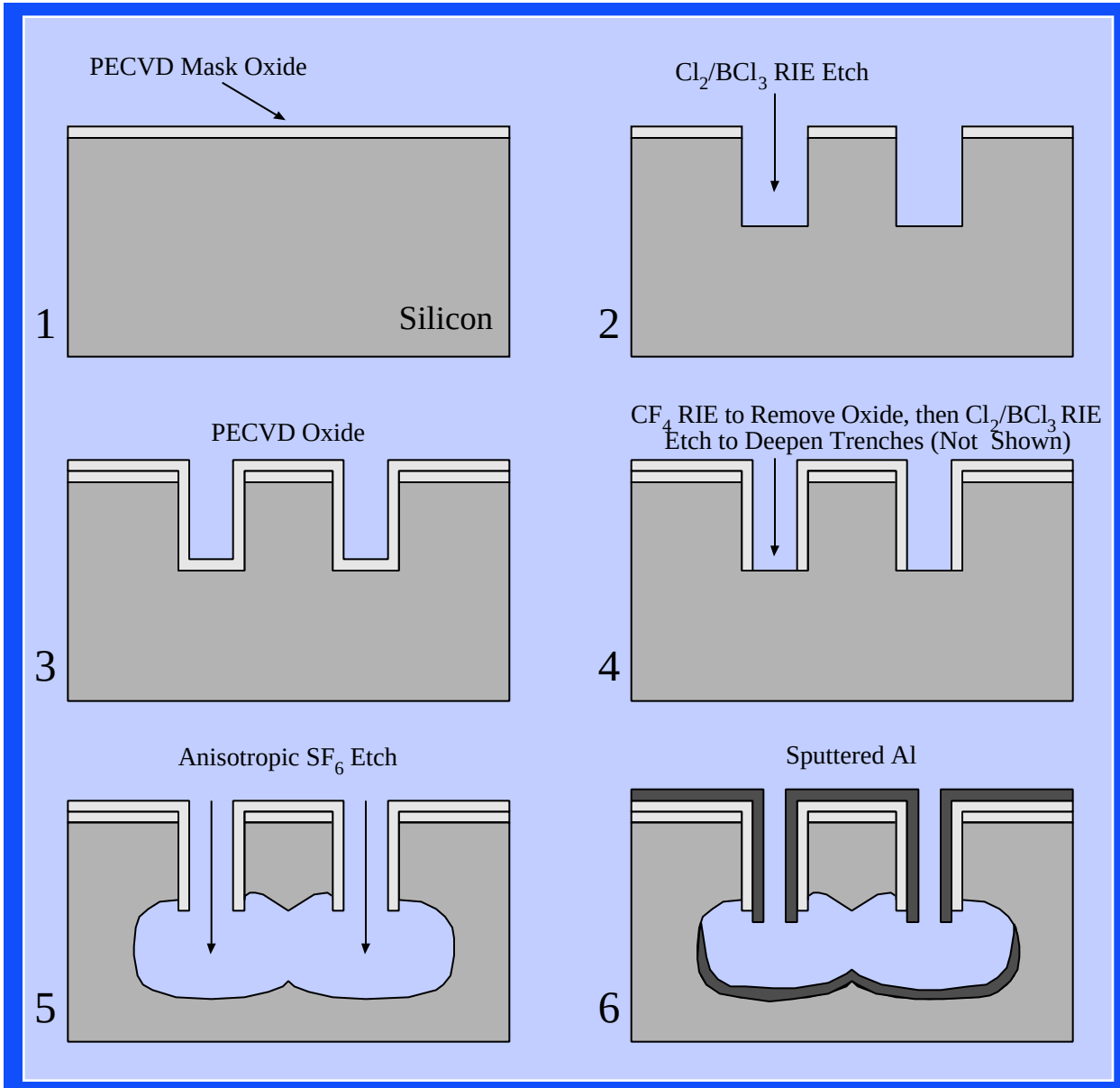
Courtesy Prof. N. Maluf, Lucas NovaSensor.

DOPANT-DEPENDENT PLASMA ETCH ISOTROPY



- **Li, et al. (1995) demonstrated markedly increased etch rates in n+ regions when using a chlorine plasma.**
- **It is theorized that since the n-doping raises the Fermi level, the energy barrier for reaction with chemisorbed Cl atoms is reduced and the more ionic nature of Si-Cl bonds in the region increases Cl chemisorption and penetration into the Si lattice.**

Li, Y. X., French, P. J., Sarro, P. M., and Wolffenbuttel, R. F., "Fabrication of a Single Crystalline Silicon Capacitive Lateral Accelerometer Using Micromachining Based on Single Step Plasma Etching," Proceedings of the IEEE Micro Electro Mechanical Systems Conference, Amsterdam, Netherlands, Jan. 29 - Feb. 2, 1995, pp. 398 - 403.

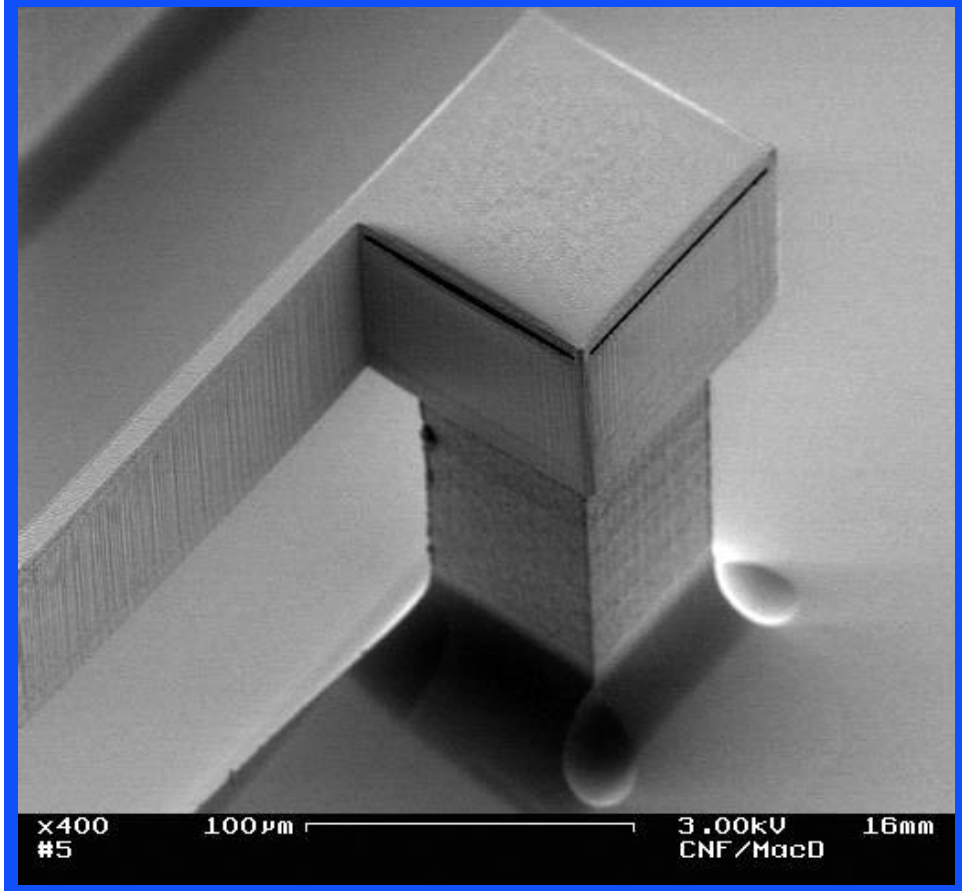


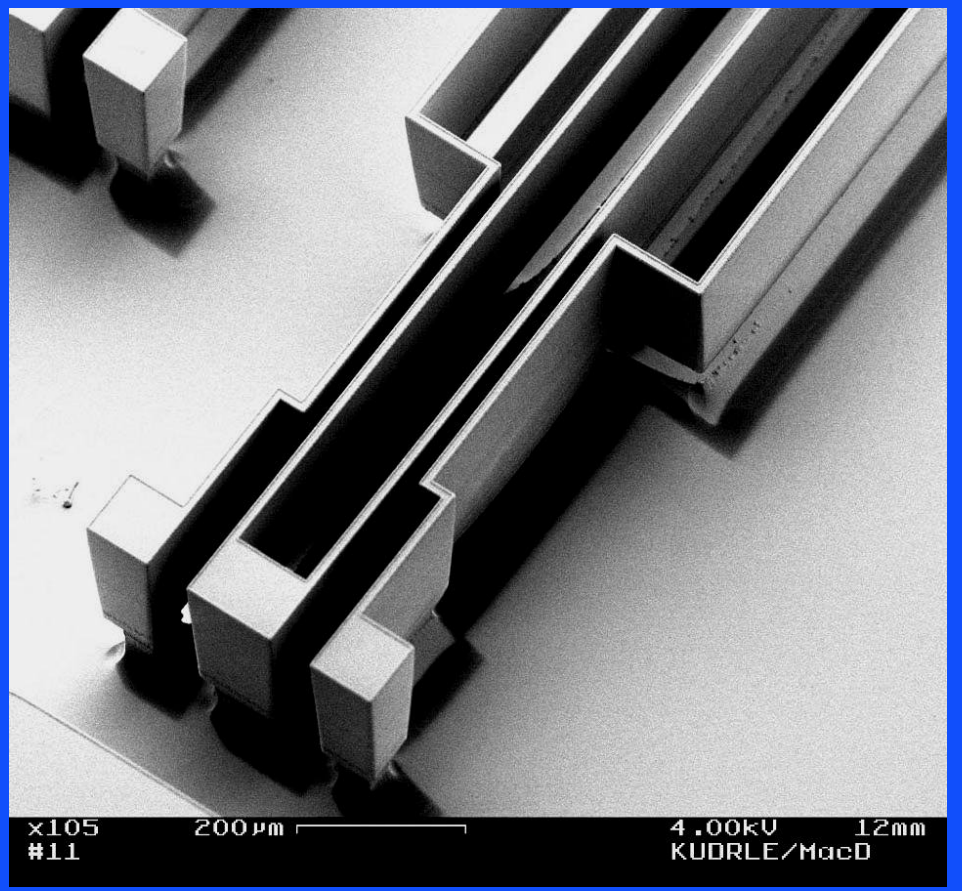
After Shaw, et al., (1993).

VARIABLE ANISOTROPY Si ETCHES

- Change reactant gases during process, changing degree of etch anisotropy.
- Can generate fully undercut structures of single-crystal silicon.

Shaw, K. A., Adams, S. G., and MacDonald, N. C., "A Single-Mask Lateral Accelerometer," Digest of Technical Papers, Transducers '93, Yokohama, Japan, June 7 - 10, 1993, pp. 210 - 213.



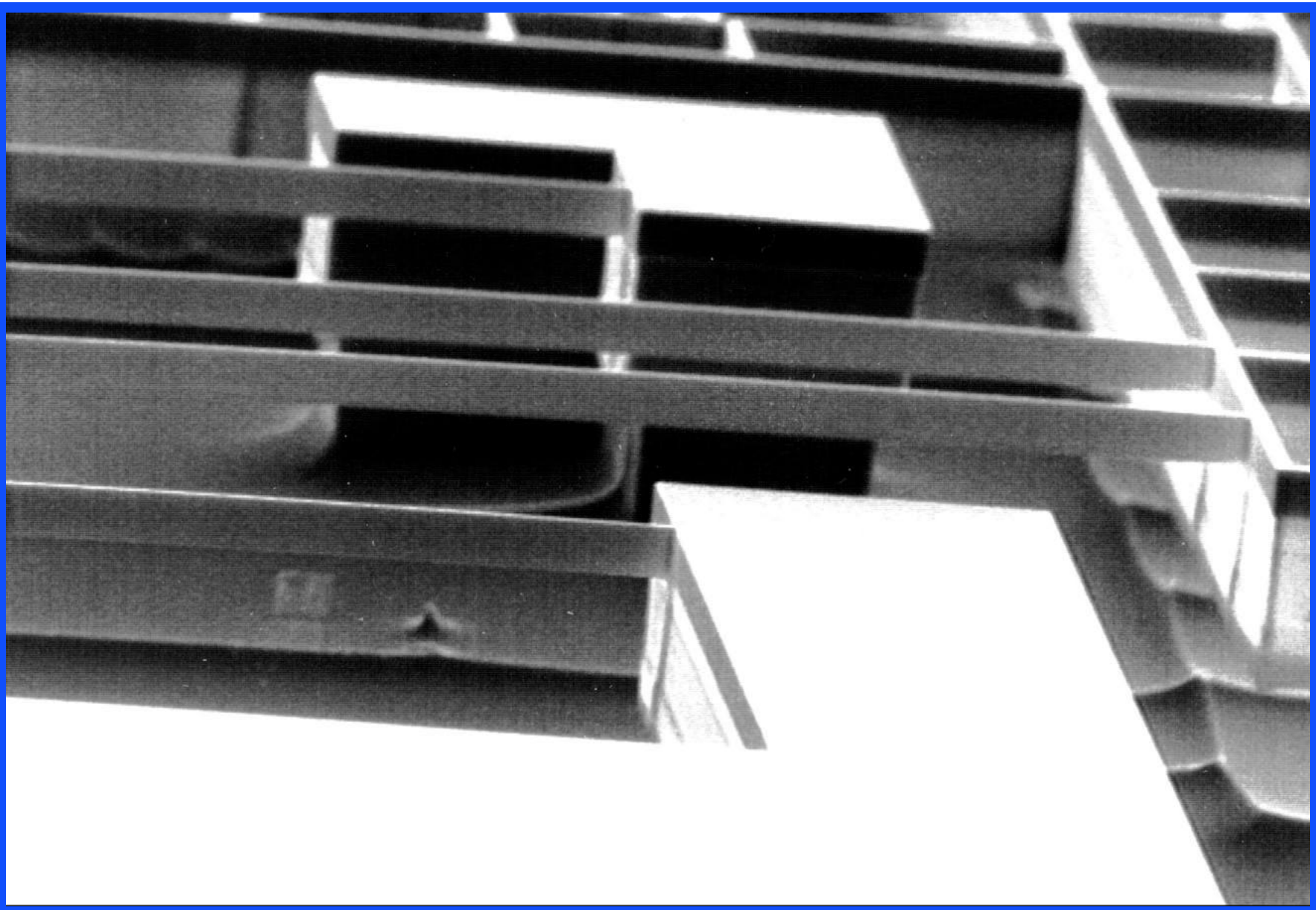


Millimeter-wave stepped impedance low-pass filter (cutoff frequency = 30 GHz).

Courtesy Dr. H. Neves and Prof. N. MacDonald, Cornell University.

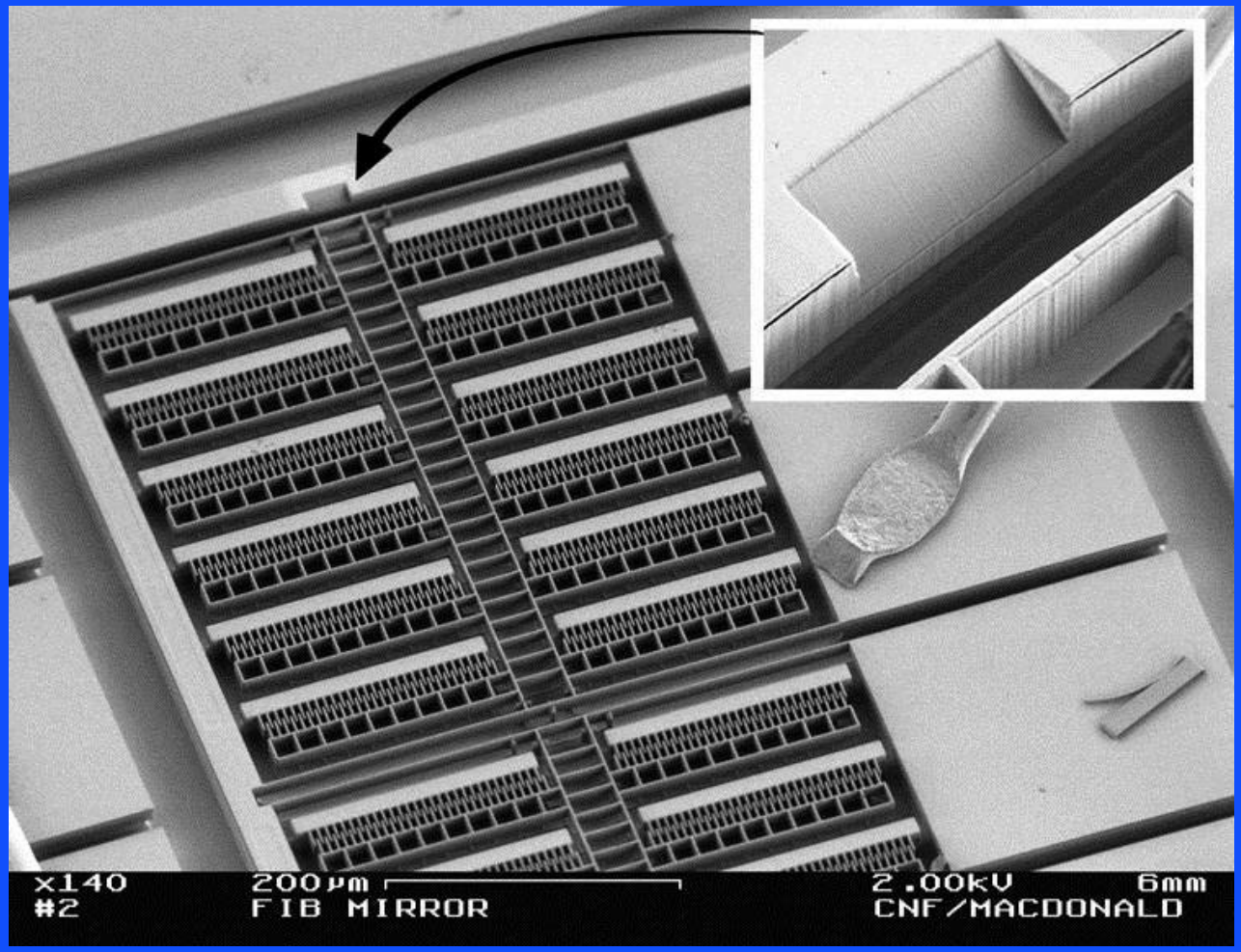
Two-depth actuator. The actuator itself is 100 microns deep, whereas the springs are only 20 microns deep. This allows large displacements (over 100 microns) at low voltages (lower than 30 volts).

Courtesy Dr. H. Neves and Prof. N. MacDonald, Cornell University.



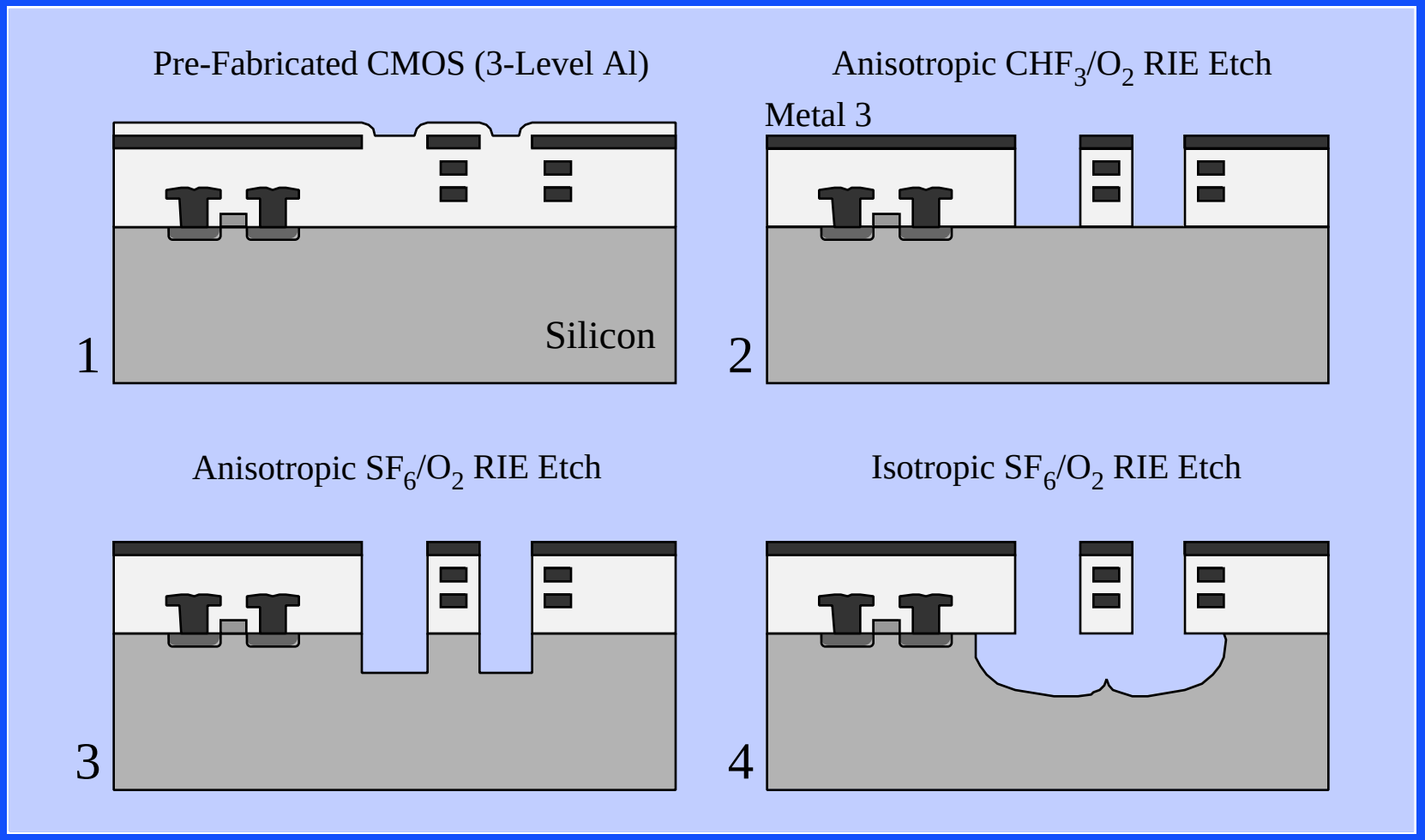
Courtesy Dr. H. Neves and Prof. N. MacDonald, Cornell University.

COMBINATION OF VARIABLE ANISOTROPY AND FOCUSED ION BEAM ETCHING

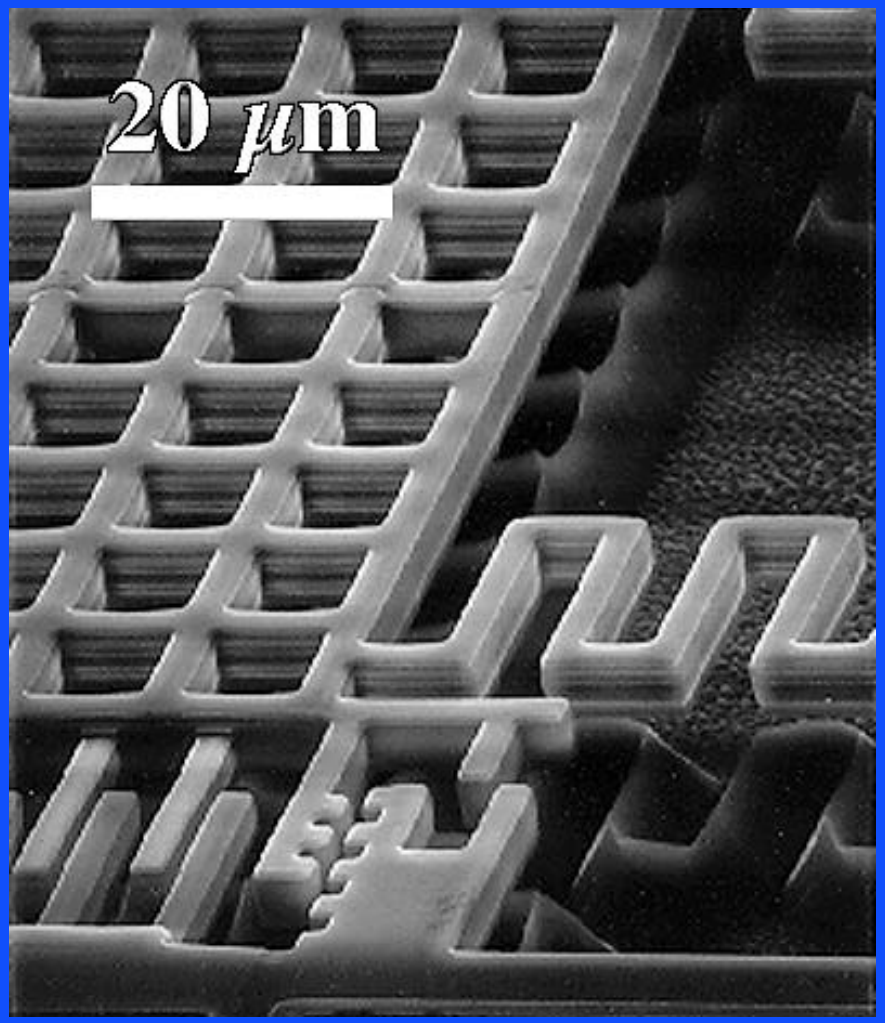


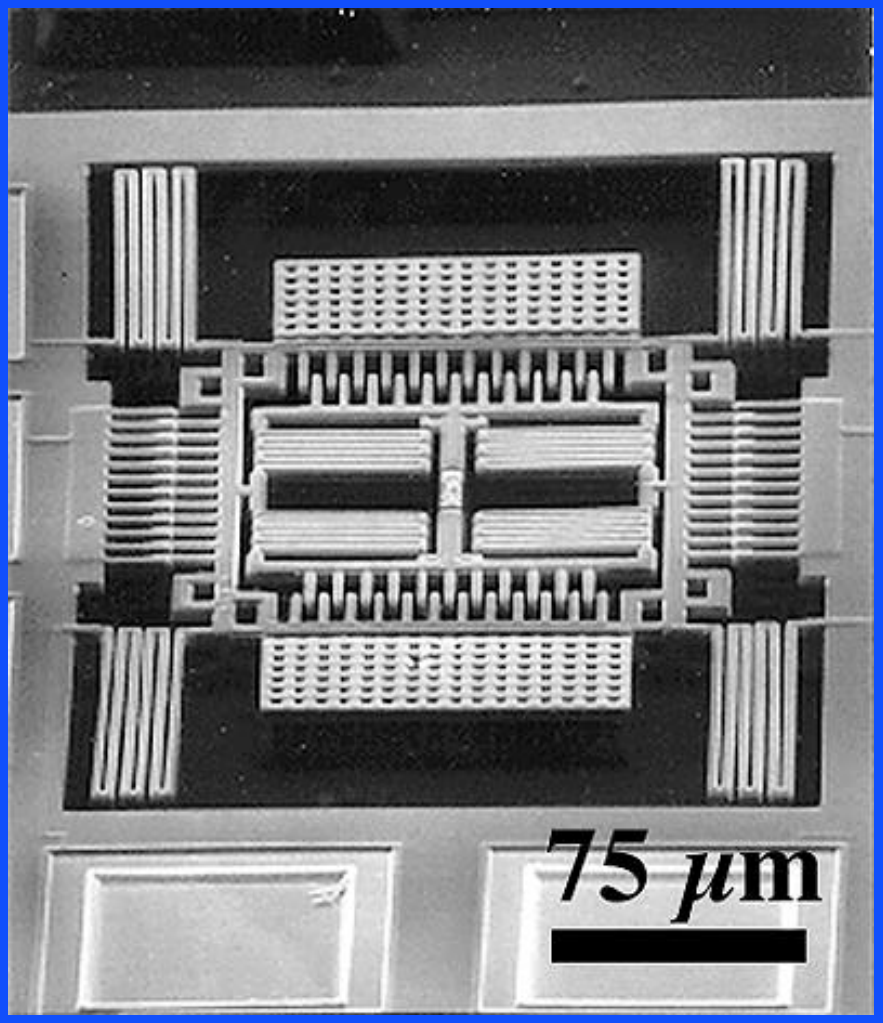
Courtesy Dr. H. Neves and Prof. N. MacDonald, Cornell University.

VARIABLE ANISOTROPY POST-PROCESSING OF CMOS



After Fedder, et al., (1996).





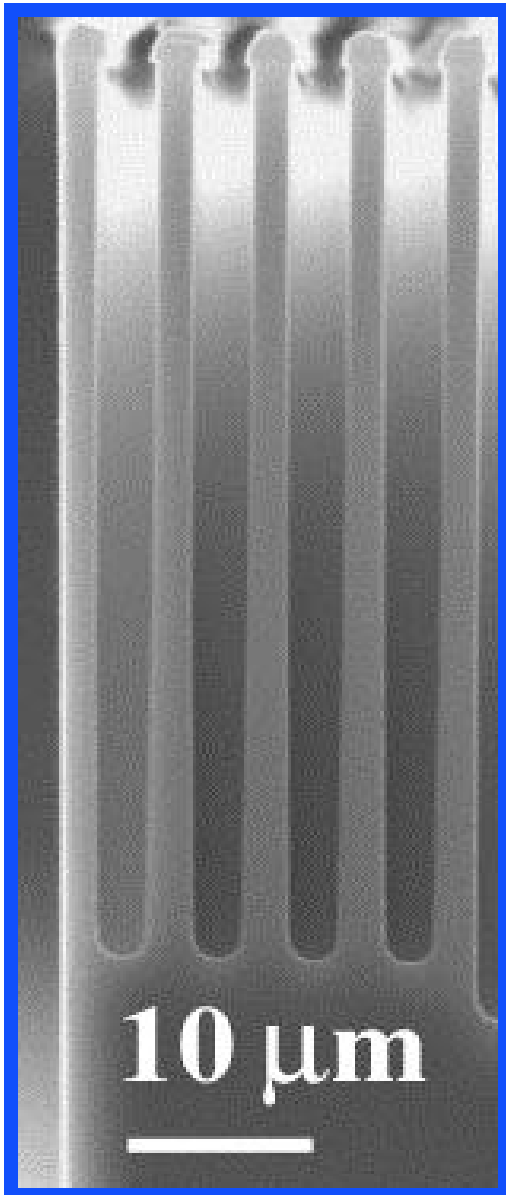
Courtesy Prof. G. Fedder, Carnegie-Mellon University.

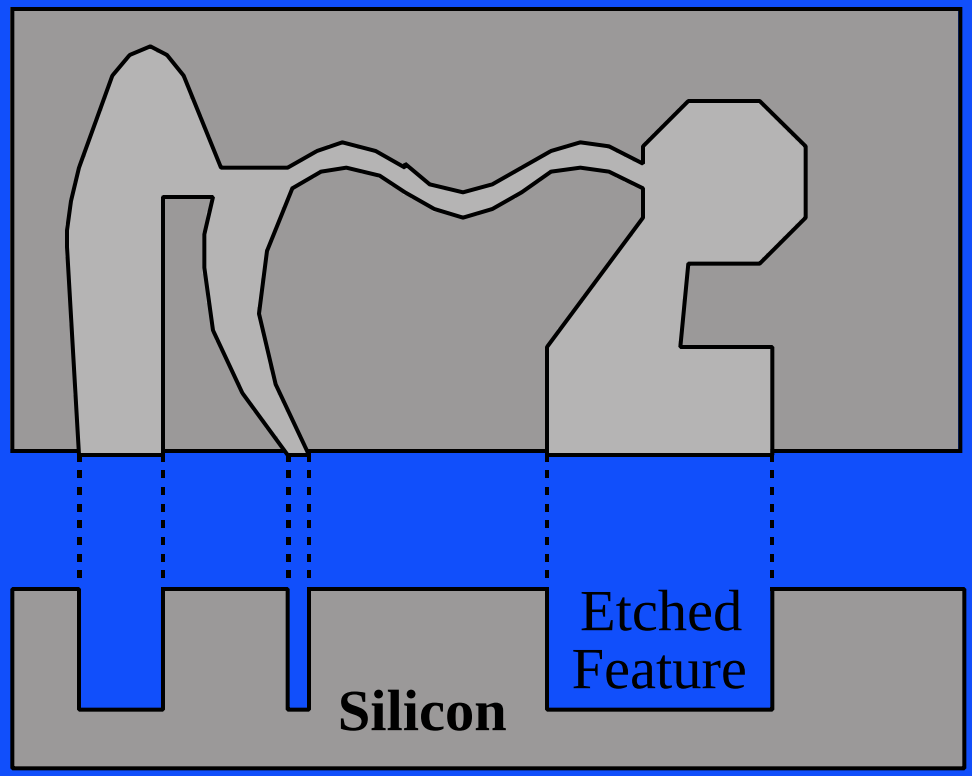
Fedder, G. K., Santhanam, S., Reed, M. L., Eagle, S. C., Guillou, D. F., Lu, M. S.-C., and Carley, L. R., "Laminated High-Aspect-Ratio Microstructures in a Conventional CMOS Process," Proceedings of IEEE International Workshop on Micro Electro Mechanical Systems, San Diego, CA, Feb. 11 - 15, 1996, pp. 13 - 18.

DEEP REACTIVE ION ETCHING (DRIE)

- DRIE is a variant of RIE in which the process gases are changed between one optimized for silicon etching and one optimized for sidewall passivation.
- This technology was invented by Lärmer and Schilp (patent issued 1994) of Bosch, Inc., in Germany.
- Typical gases are SF_6 for etching and C_4F_8 for passivation.
- Ion bombardment due to a small bias voltage during passivation essentially removes any of the ≈ 50 nm passivation layer on vertical surfaces.
- Aspect ratios greater than 30:1 are possible, with photoresist selectivities of 50 - 100:1, and SiO_2 selectivities of 120 - 200:1 being typical.
- A variety of commerical vendors sell such etchers, notably STS and Plasma-Therm.

DRIE ALLOWS ARBITRARY "NEGATIVE EXTRUSIONS"



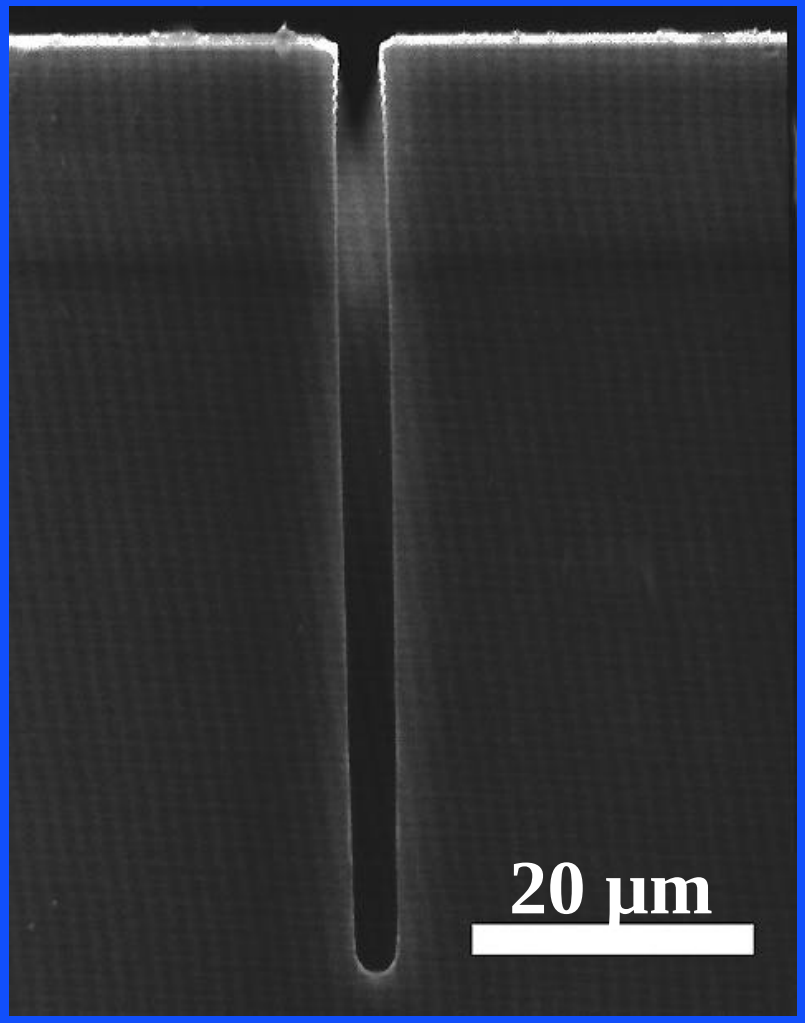


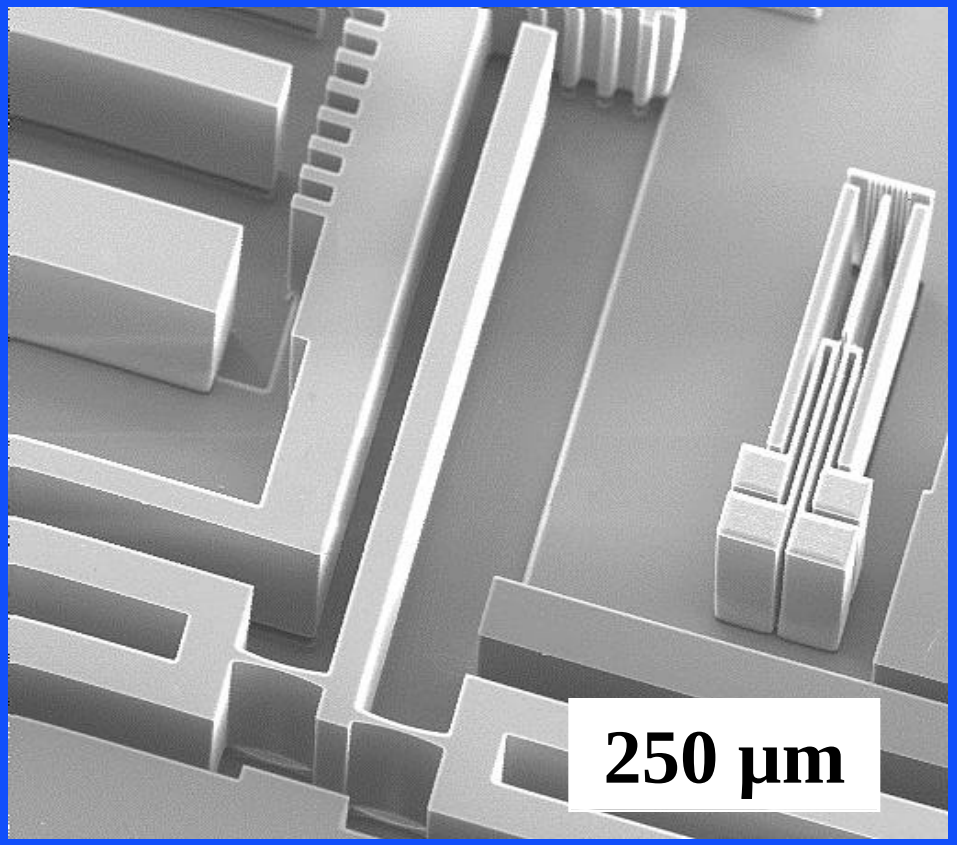
Top View

Side View

Reference: Lärmer, F., and Schilp, P., "Method of Anisotropically Etching Silicon," German Patent No. DE 4,241,045, issued 1994.

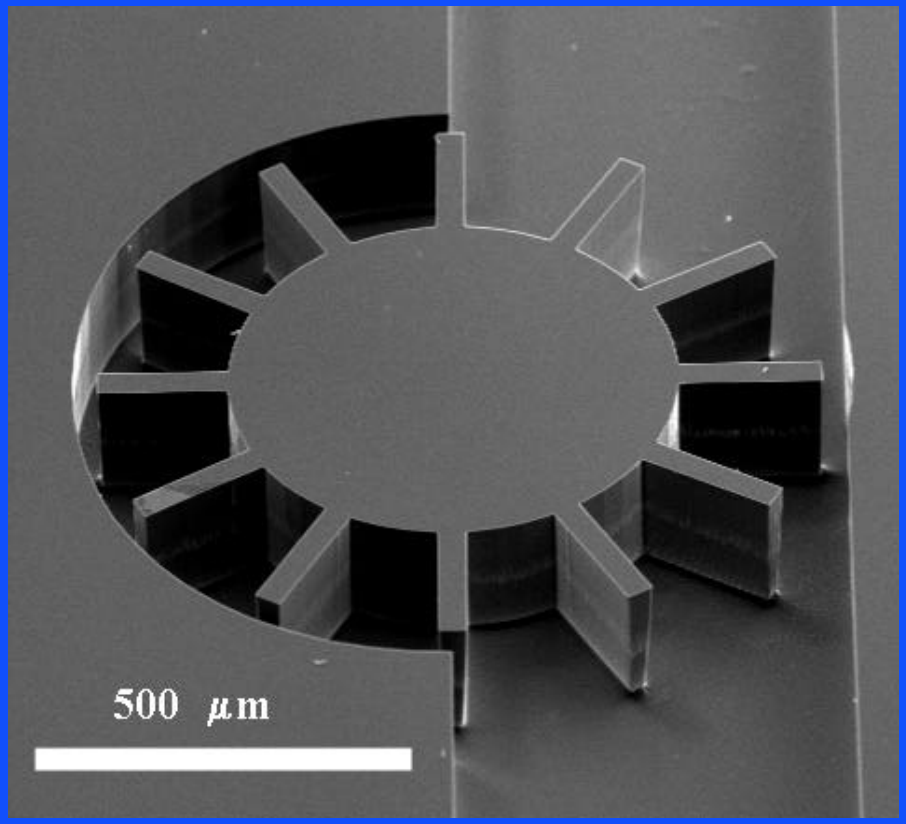
DEEP RIE EXAMPLES

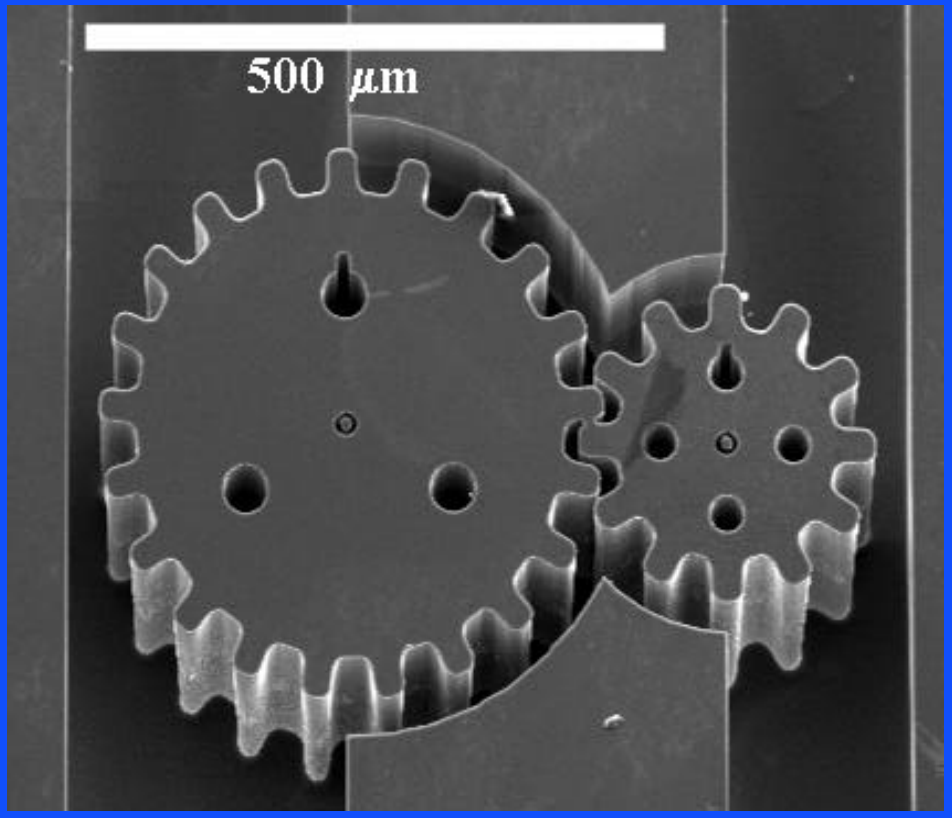




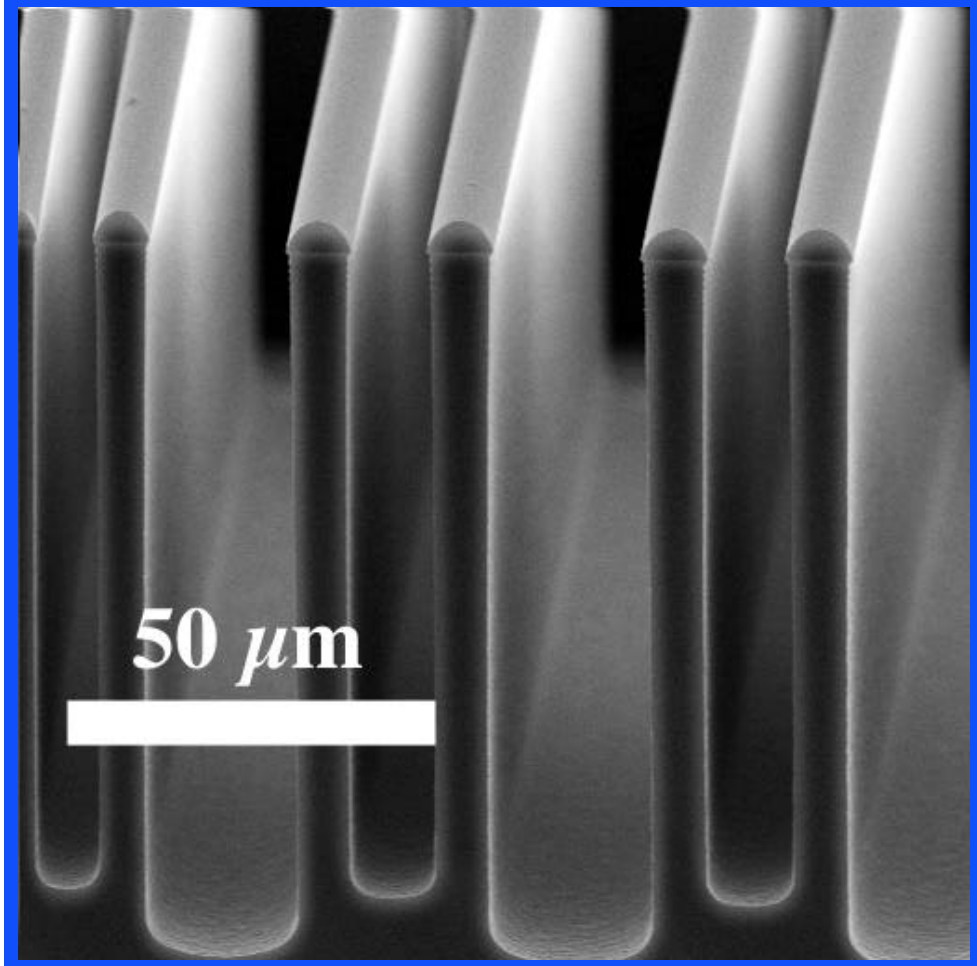
Reference: Klaassen, E. H., Petersen, K., Noworolski, J. M., Logan, J., Maluf, N. I., Brown, J., Storment, C., McCulley, W., and Kovacs, G. T. A., "Silicon Fusion Bonding and Deep Reactive Ion Etching; A New Technology for Microstructures," Digest of Technical Papers from Transducers '95/Eurosensors IX, Vol. 1, June 25 - 29, 1995, Stockholm, Sweden, pp. 556 - 559.

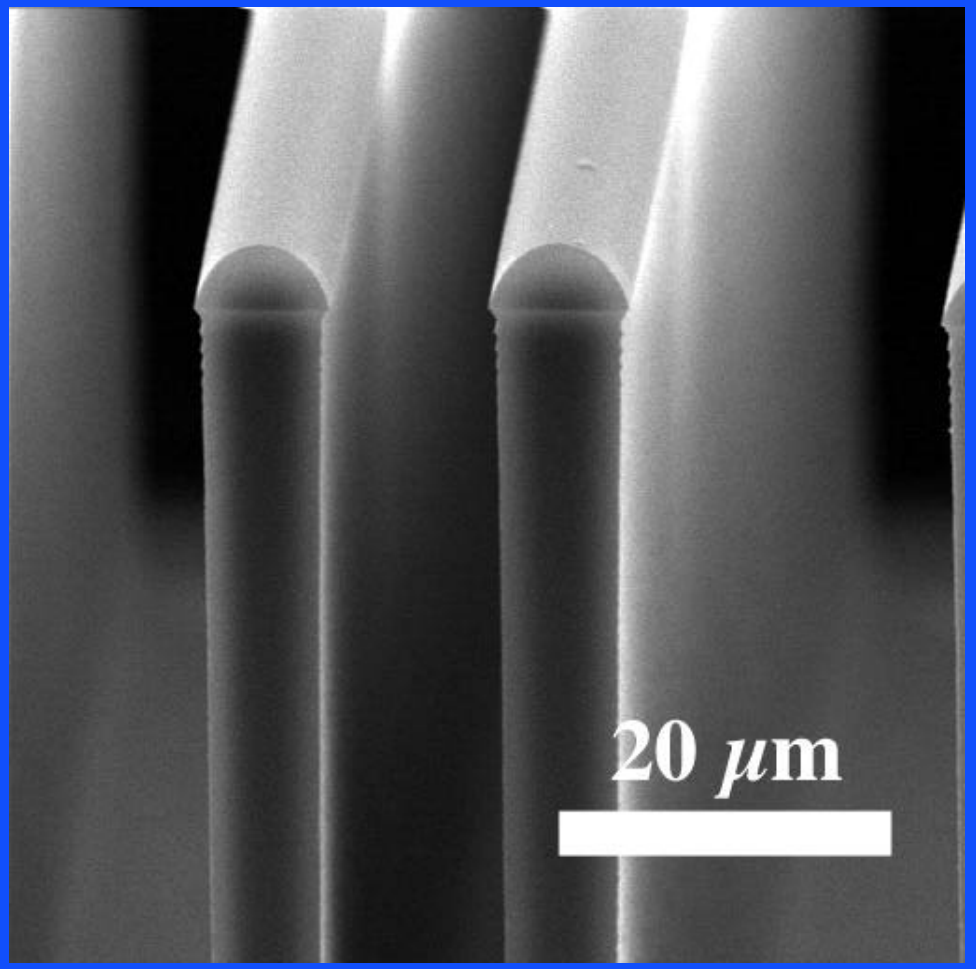
DRIE EXAMPLES



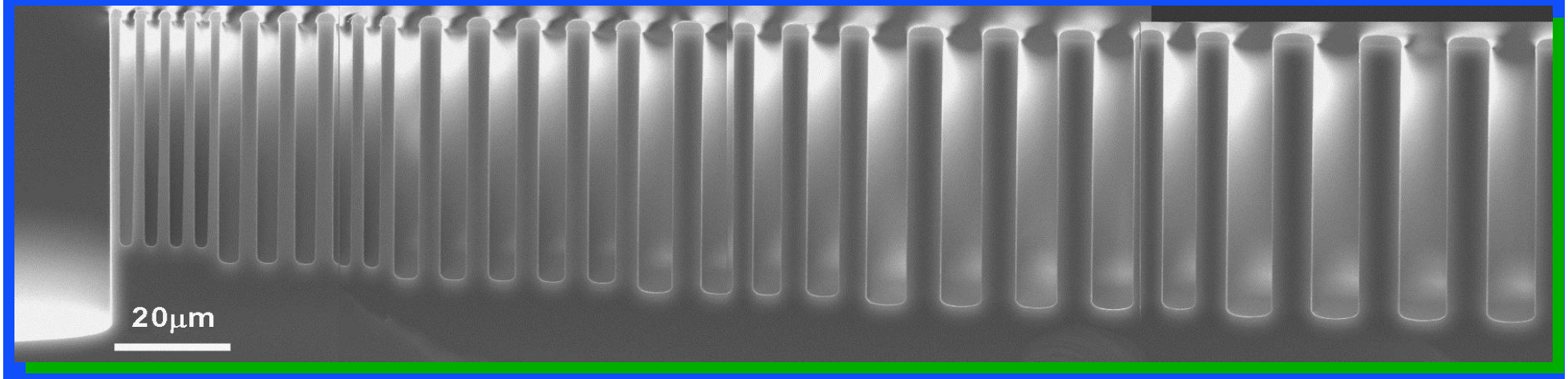


Courtesy Prof. Nadim Maluf, Lucas NovaSensor.





DRIE LOADING EFFECTS



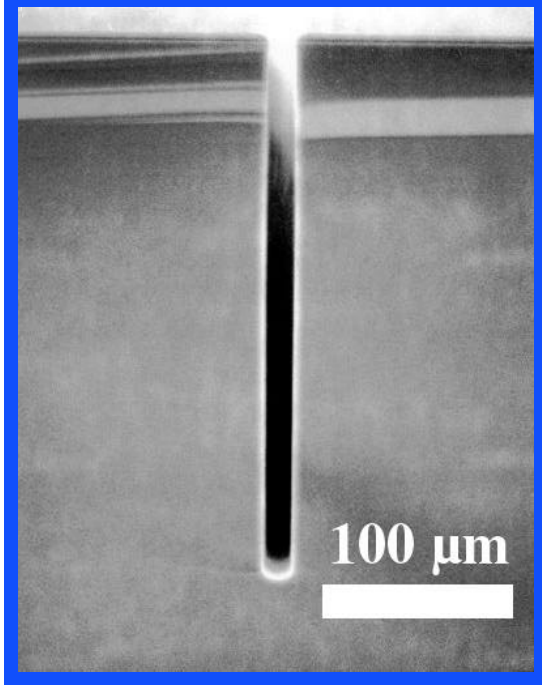
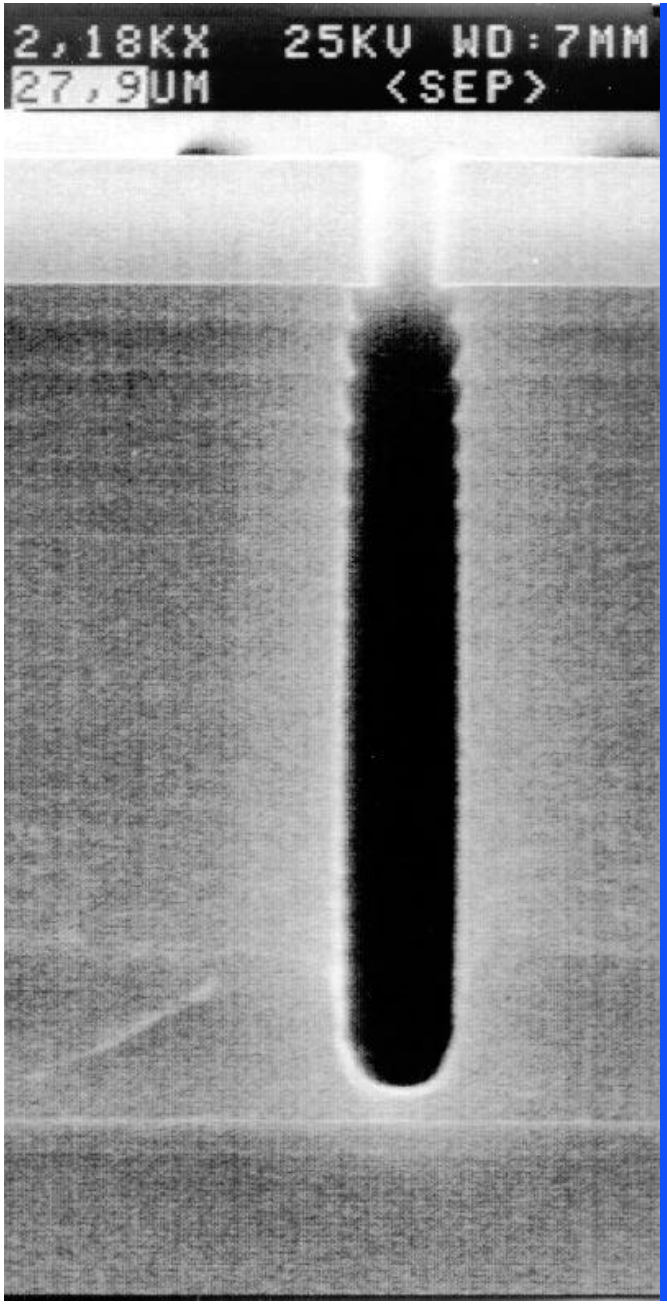


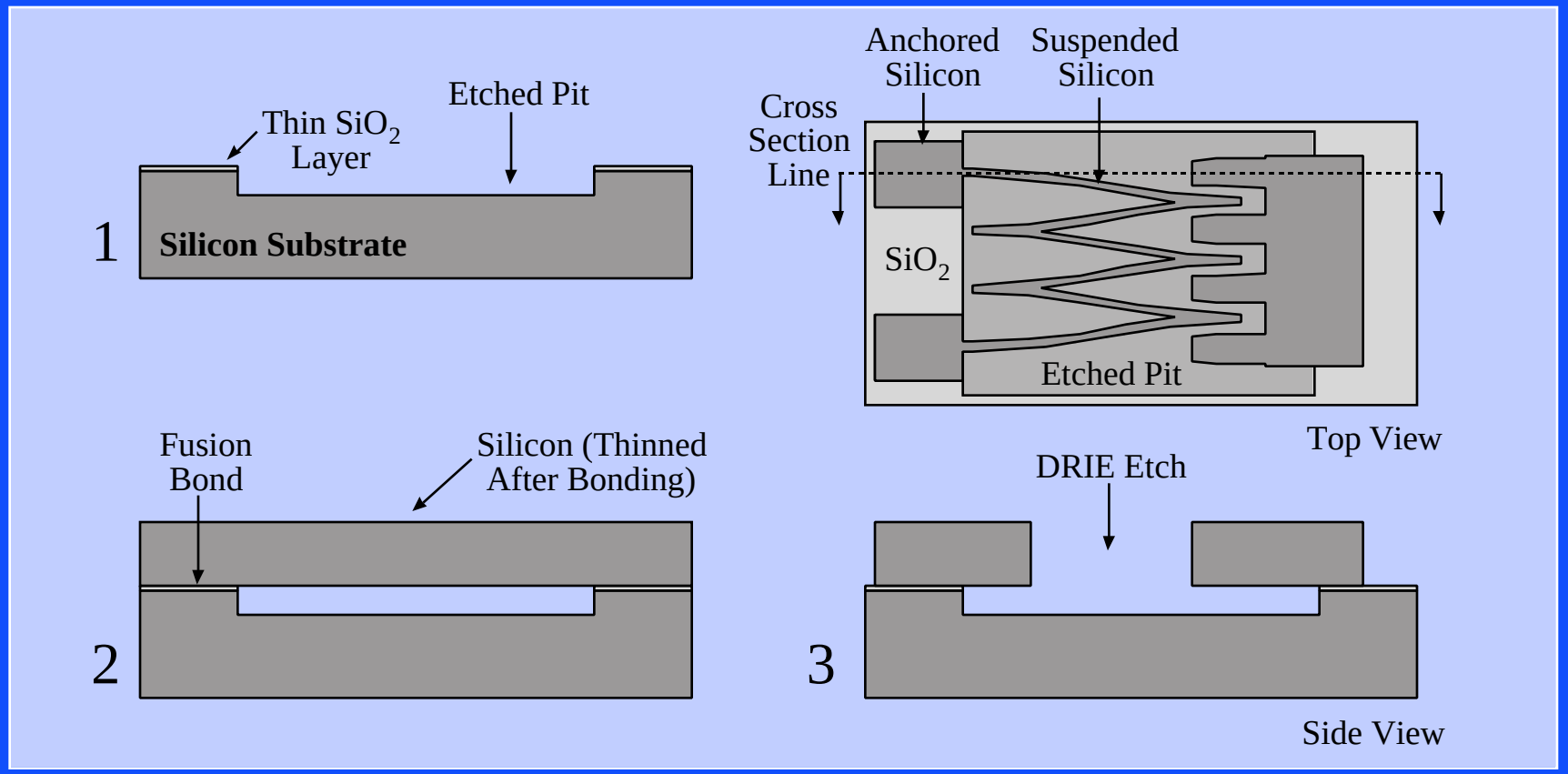
Image at left courtesy STS, Inc., Wales, UK.



SCALLOPING IN DRIE

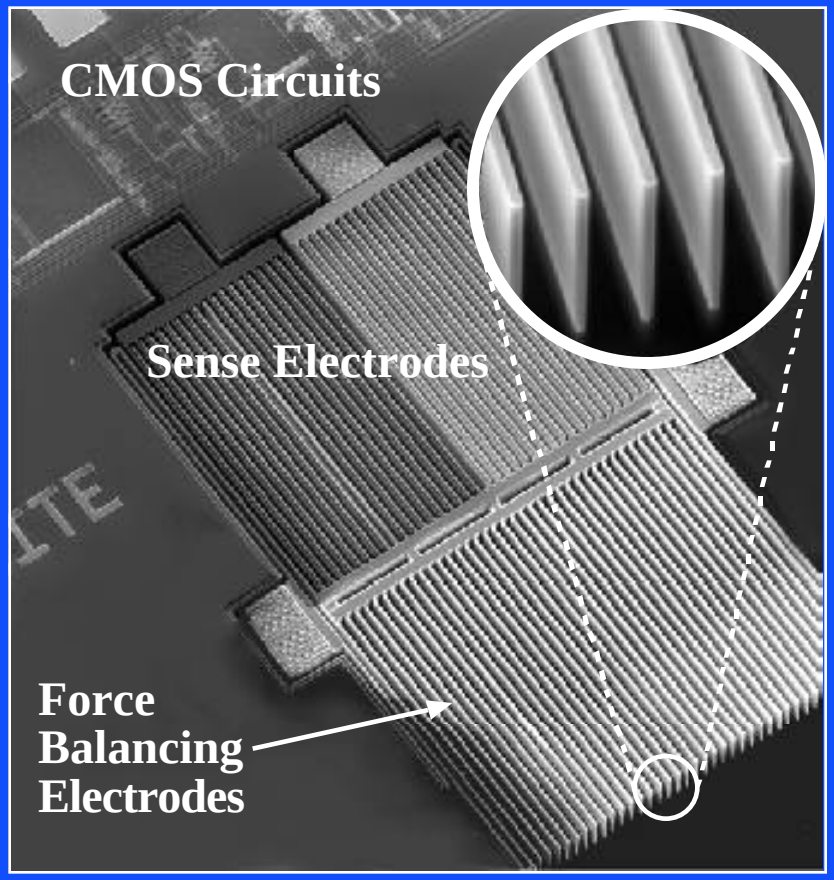
Courtesy STS, Inc., Wales, UK.

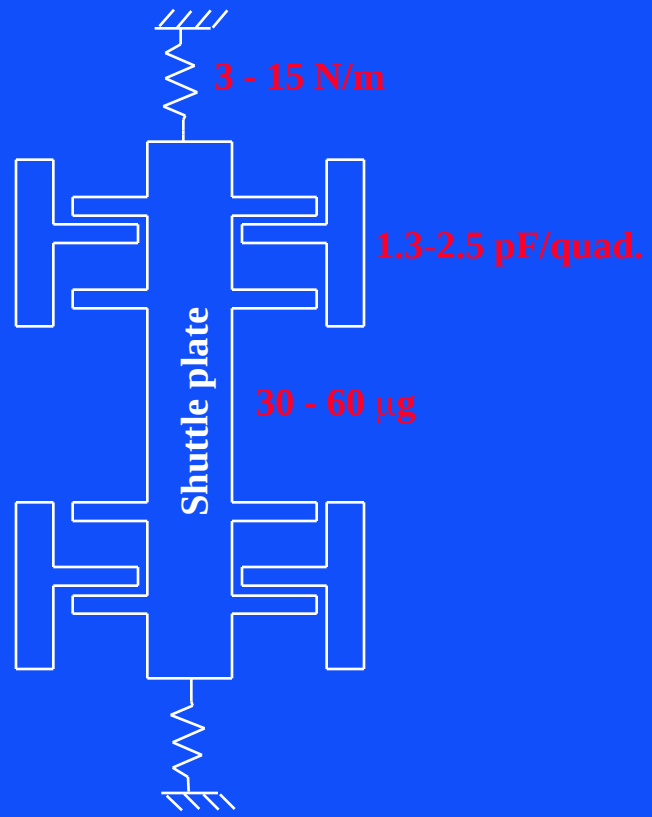
DRIE + FUSION BONDING FOR MECHANISMS



Reference: Klaassen, E. H., Petersen, K., Noworolski, J. M., Logan, J., Maluf, N. I., Brown, J., Storment, C., McCulley, W., and Kovacs, G. T. A., "Silicon Fusion Bonding and Deep Reactive Ion Etching; A New Technology for Microstructures," Digest of Technical Papers from Transducers '95/Eurosensors IX, Vol. 1, June 25 - 29, 1995, Stockholm, Sweden, pp. 556 - 559.

INTEGRATED DRIE CMOS ACCELEROMETER



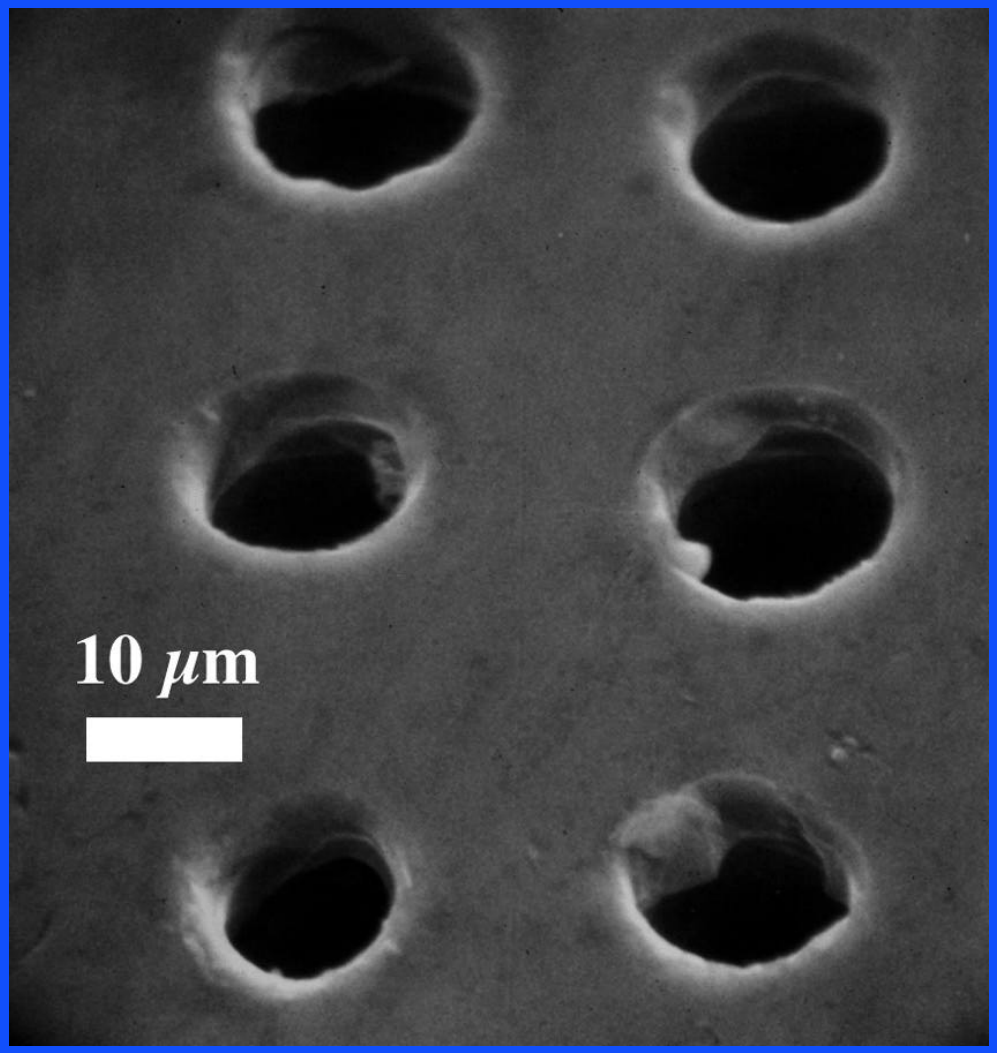


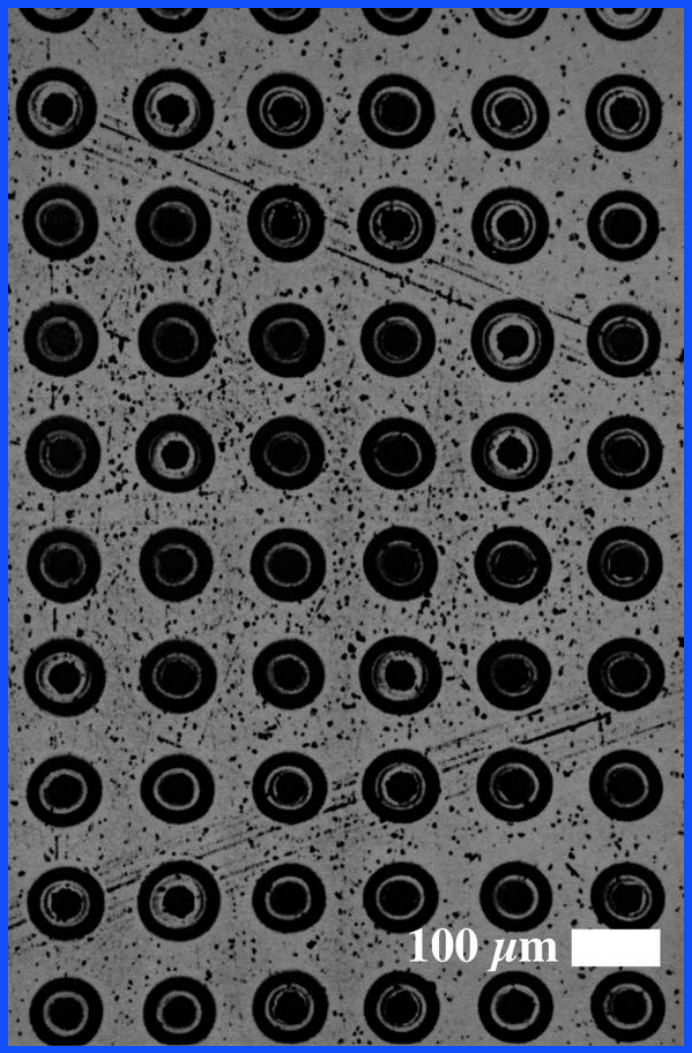
Mohan, J., Maluf, N. I., Petersen, K. E., and Kovacs, G. T. A., "An Integrated Accelerometer as a Demonstration of a New Technology Using Silicon Fusion Bonding and Deep Reactive Ion Etching," Late News Supplement, Solid-State Sensor and Actuator Workshop, Hilton Head Island, SC, June 3 - 6, 1996, pp. 21 - 22.

LASER DRILLING

- **Laser drilling is a serial processes, but it is sometimes necessary for materials where there are no suitable etches or where plasma/RIE is not an option.**
- **Laser drilling is an ablative process that can significantly damage the material being drilled.**

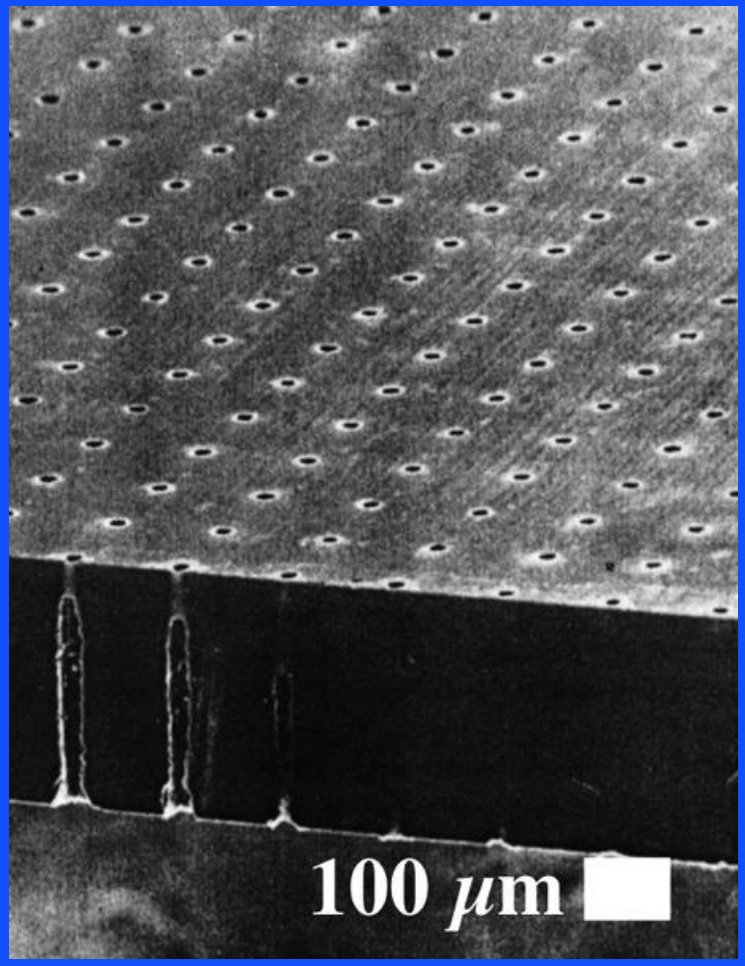
LASER DRILLING

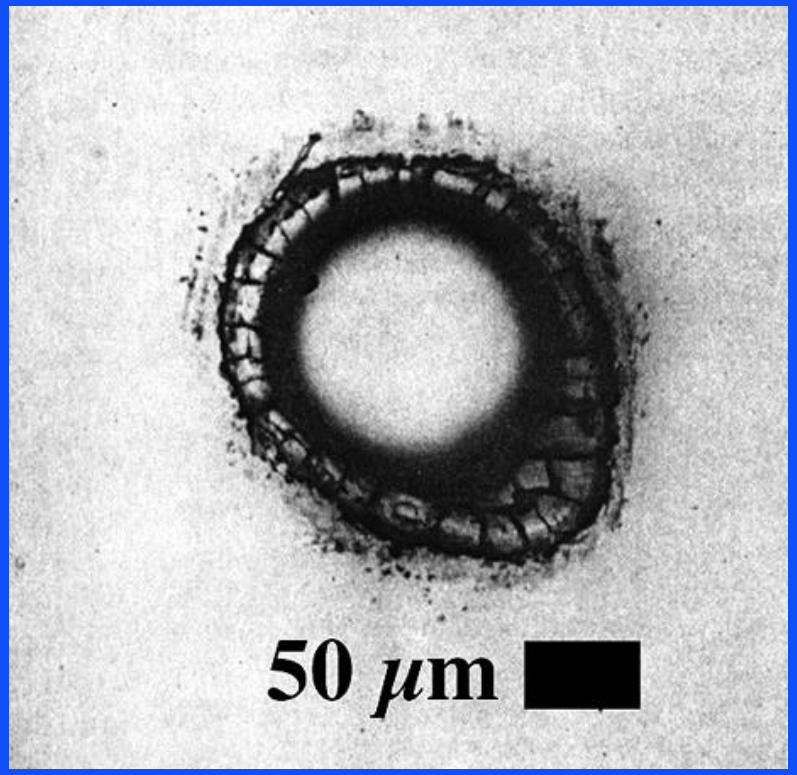




Images courtesy Dr. T. Anthony, General Electric, Inc.

LASER DRILLING DAMAGE



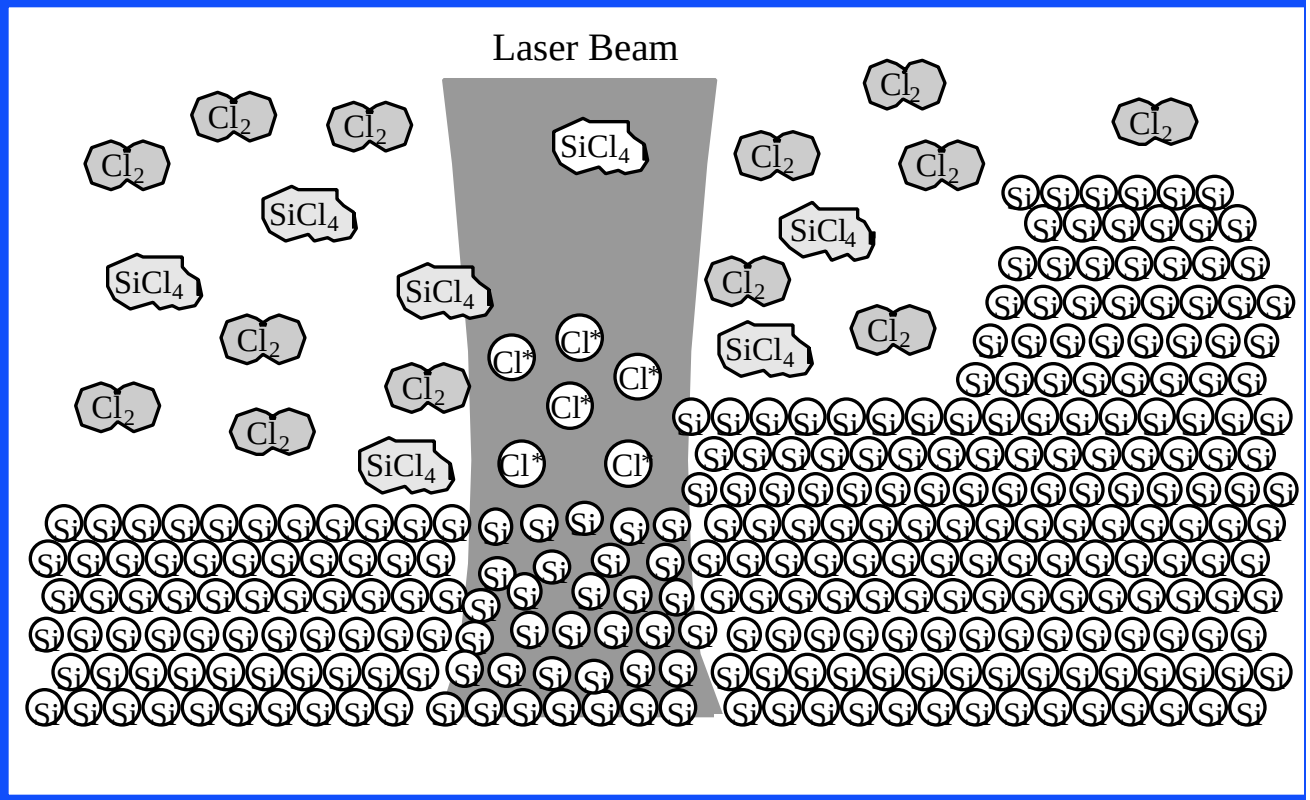


Images courtesy Dr. T. Anthony, General Electric, Inc.

Reference: Anthony, T. R., "Forming Feedthroughs in Laser-Drilled Holes in Semiconductor Wafers by Double-Sided Sputtering," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, vol. CHMT-5, no. 1, Mar. 1982, pp. 171 - 180.

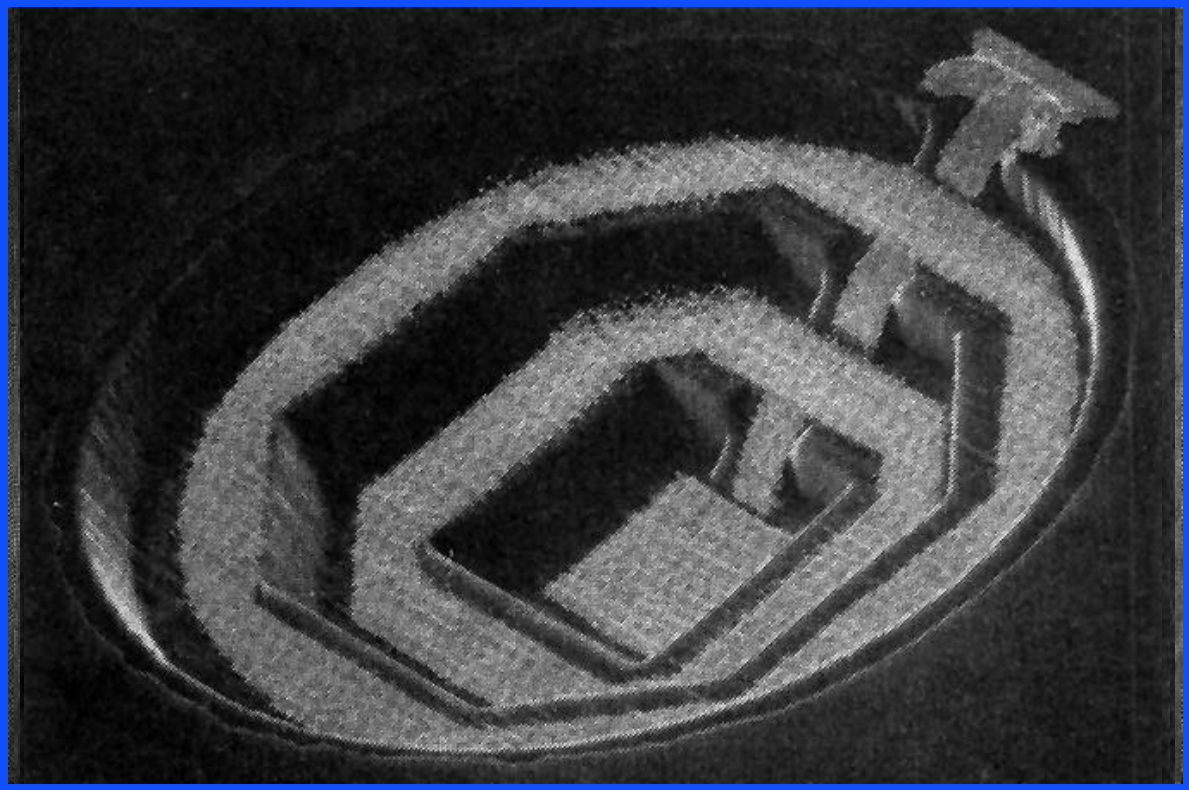
LASER ASSISTED CHEMICAL ETCHING

- **Laser-assisted chemical etching (LACE) uses localized heating to drive etching reactions.**
- **It is a serial processes, but is sometimes necessary.**
- **LACE can be very slow but can offer 1 μm^3 voxel resolution.**

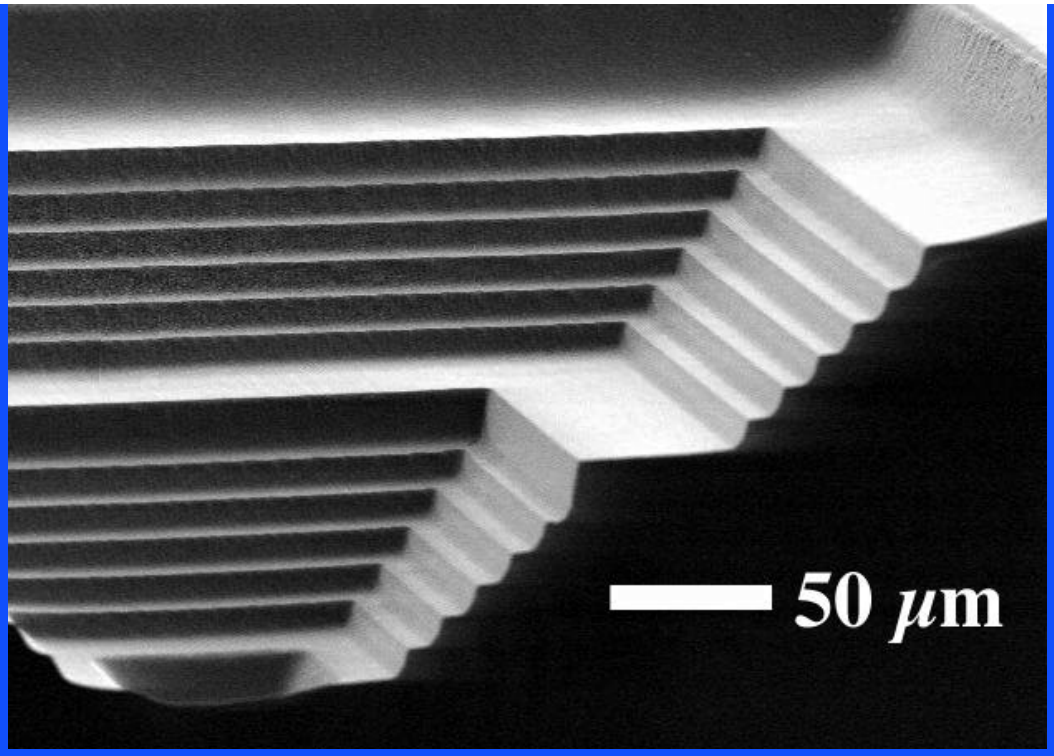


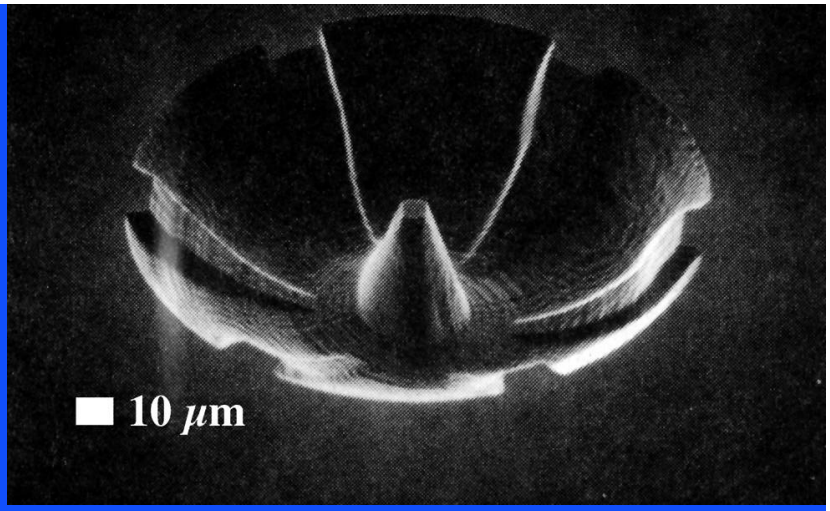
After Bloomstein and Ehrlich (1991).

Bloomstein, T. M., and Ehrlich, D. J., "Laser Deposition and Etching of Three-Dimensional Microstructures," Proceedings of Transducers '91, the 1991 International Conference on Solid-State Sensors and Actuators Digest of Technical Papers, IEEE Press, San Francisco, CA, June 24 - 27, 1991, pp. 507 - 511.



Source: Bloomstein, T. M., and Ehrlich, D. J., "Laser Deposition and Etching of Three-Dimensional Microstructures," Proceedings of Transducers '91, the 1991 International Conference on Solid-State Sensors and Actuators Digest of Technical Papers, IEEE Press, San Francisco, CA, June 24 - 27, 1991, pp. 507 - 511.





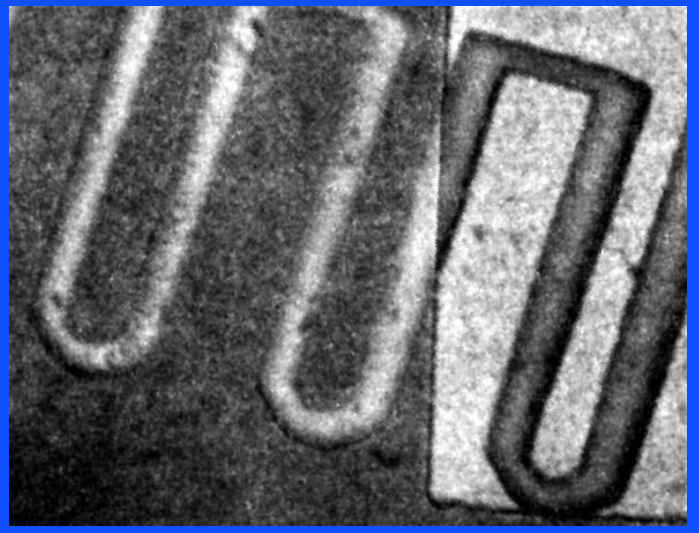


Image courtesy of Revise, Inc., Cambridge, MA.

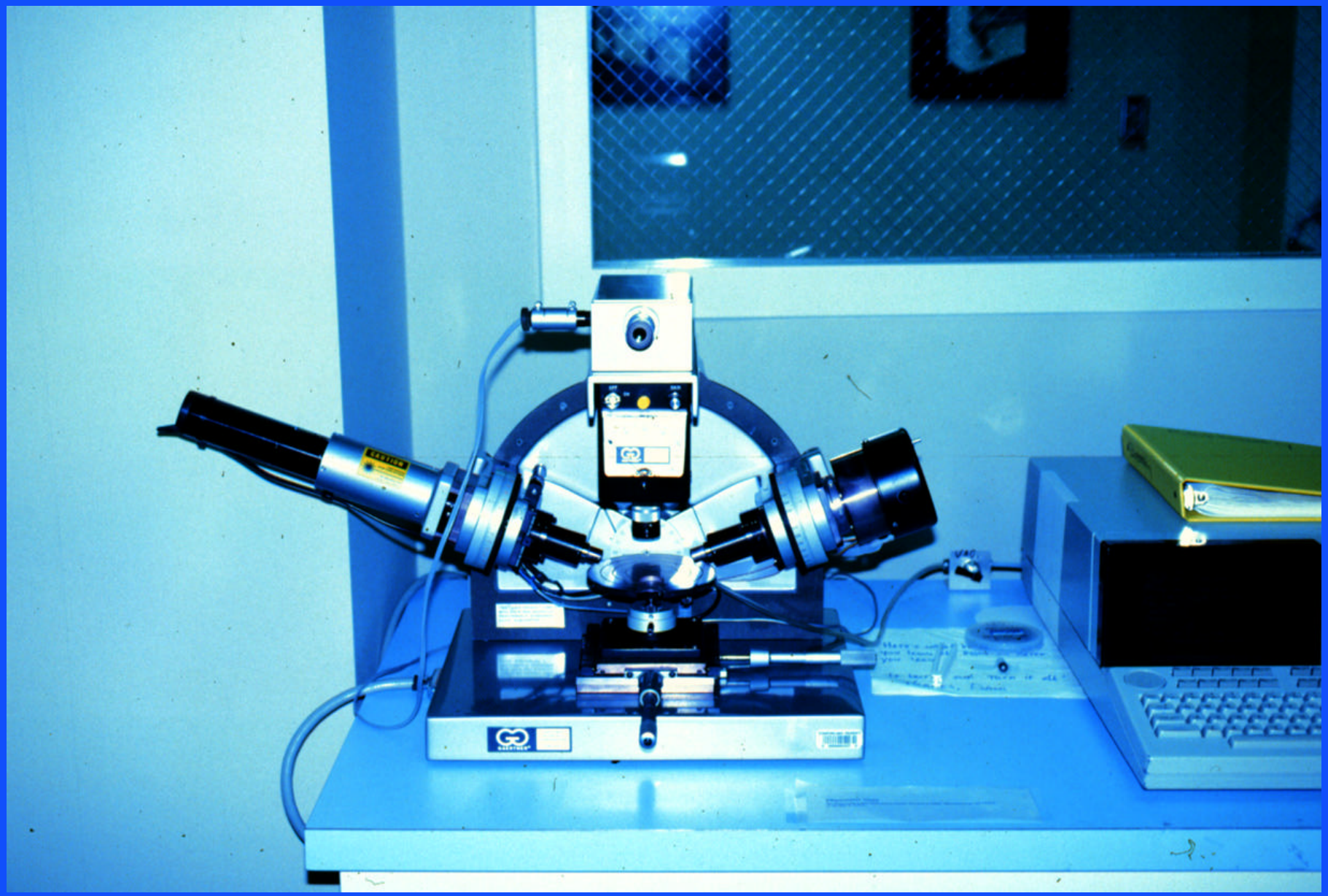
Material	Coefficient of Thermal Expansion 10^{-6}/K	Young's Modulus GPa	Thermal Conductivity W/m•K	Density g/cm^3
Si	2.33 [2] 2.6 [4]	190 [2] 162 [4]	149 [2] 170 [4]	2.3 [2] 2.42 [4]
SiO_2	0.4 [4]	92 (sputtered) [1] 67 (dry) [1] 57 (wet) [1] 70 (bulk) [1]	1.4 [4]	2.66 [4] 2.3 (plasma) [6]
Si_3N_4	2.8 [4]	146 (CVD) [1] 130 (sputtered) [1]	18.5 [4]	3.44 [4] 2.9 to 3.1 (LPCVD) [6] 2.4 to 2.8 (PECVD) [6]
Poly-Si	2.33 [4]	150 [5]	20 to 30 [3]	2.33 [4]
Polyimide (PIQ L200, Hitachi)	2.0 [7]	8.63 [7]	-	-
Polyimide (PIQ 3200, Hitachi)	54 [7]	2.95 [7]	-	-
Aluminum	23.0 [4]	69 [4]	236 [2] 234 [4]	2.7 [2] 2.692 [4]
Gold	14.3 [4]	80 [4]	318 [4]	19.4 [4]
Platinum	8.9 [4]	147 [4]	73 [4]	21.4 [4]
Nickel	12.8 [4]	210 [4]	90.9 [4]	9.04 [4]

PROPERTIES OF EXAMPLE THIN FILMS

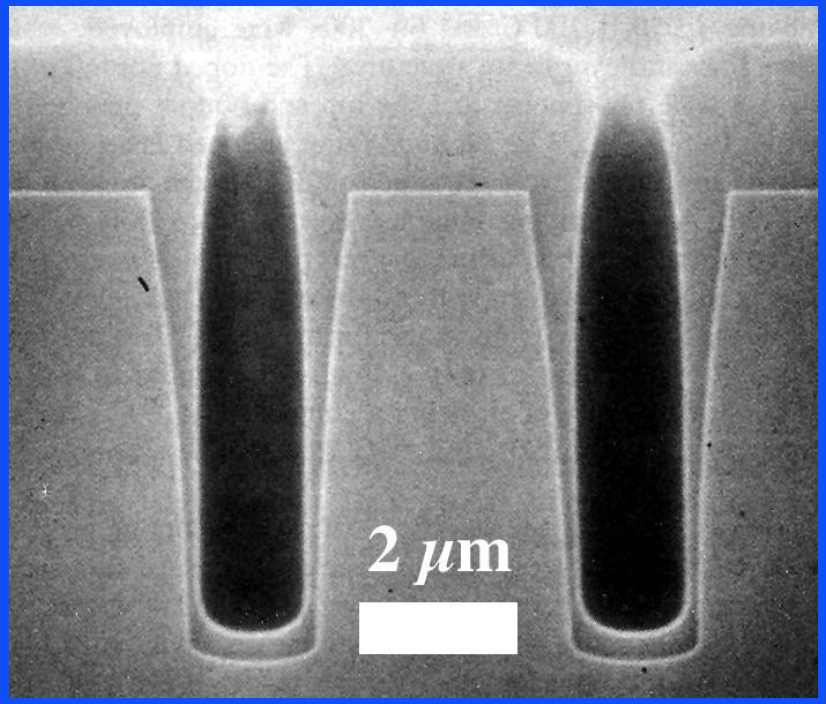
Table of material properties for general comparison (to be used cautiously, since some are for bulk materials). From Petersen (1978) [1], Petersen (1982) [2], Lenggenhager (1994) [3], Riethmüller and Benecke (1988) [4], Tang, et al. (1990) [5], Sze (1988) [6], and Suh, et al. (1996) [7]. A diverse database of such properties that illustrates their wide variations can be found at http://mems.isi.edu/mems/materials.

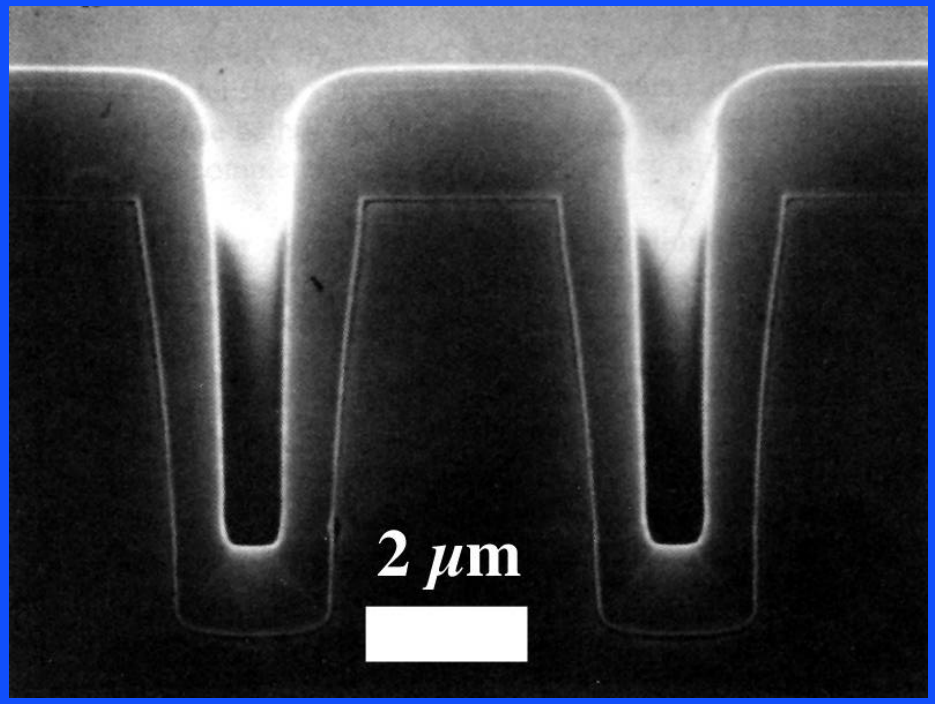
THIN FILM DEPOSITION AND ETCHING

- **Chemical vapor deposition (CVD) generally uses thermal energy to drive the reaction between reactant gases to deposit films on substrates.**
- **Plasma-Enhanced CVD (PECVD) substitutes electron bombardment for some of the thermal energy to drive the reactions, allowing greater control over stresses and other film properties.**
- **Evaporation of metal thin films is accomplished by direct heating or bombardment of a target with an electron beam.**
- **Sputtering (RF or DC) is a technique (predominantly used for metal deposition) wherein inert ions (such as Ar^+) are used to bombard a target, generating a vapor of target material (generally providing better stress control and step coverage than evaporation).**



COMPARISON OF LPCVD AND PECVD DEPOSITION OF PSG





LPCVD SiH_4, O_2, PH_3, 425°C, 280 mTorr.

PECVD TEOS, TMP, O_2.

Source: Ristic, Lj., [ed.], "Sensor Technology and Devices, Artech House, 1994.

SILICON DIOXIDE

- **The most commonly available dielectric in silicon fabrication facilities.**
- **Does not block alkali ions.**
- **Can be grown in situ or deposited (CVD, LPCVD, PECVD, sputtering, etc.).**
- **Properties vary widely depending upon deposition method.**
- **Stress is only controllable "at will" for PECVD.**

Deposition Type	Plasma	SiH_4 + O2	TEOS	$SiCl_2H_2$ + N_2O	Native Oxide (thermal)
Typical Temp.	200° C	450° C	700° C	900° C	1100° C
Composition	$SiO_{1.9}$(H)	SiO_2(H)	SiO_2	SiO_2(Cl)	SiO_2
Step Coverage	Varies (Sze says nonconformal)	Nonconformal	Conformal	Conformal	Conformal
Thermal Stability	loses H	densifies	stable	loses Cl	excellent
Density (g/cm^3)	2.3	2.1	2.2	2.2	2.2
Refractive Index	1.47	1.44	1.46	1.46	1.46
Stress (10^9 dyn/cm^2)	3 comp - 3 tens	3 tens	1 comp	3 comp	some comp
Dielectric Strength (10^6 V/cm or 10^2V/μm)	3-6	8	10	10	10
Etch Rate (Å/min) (100:1 H_2O:HF)	400	60	30	30	≈ 30

Reference: Adams (1983)...

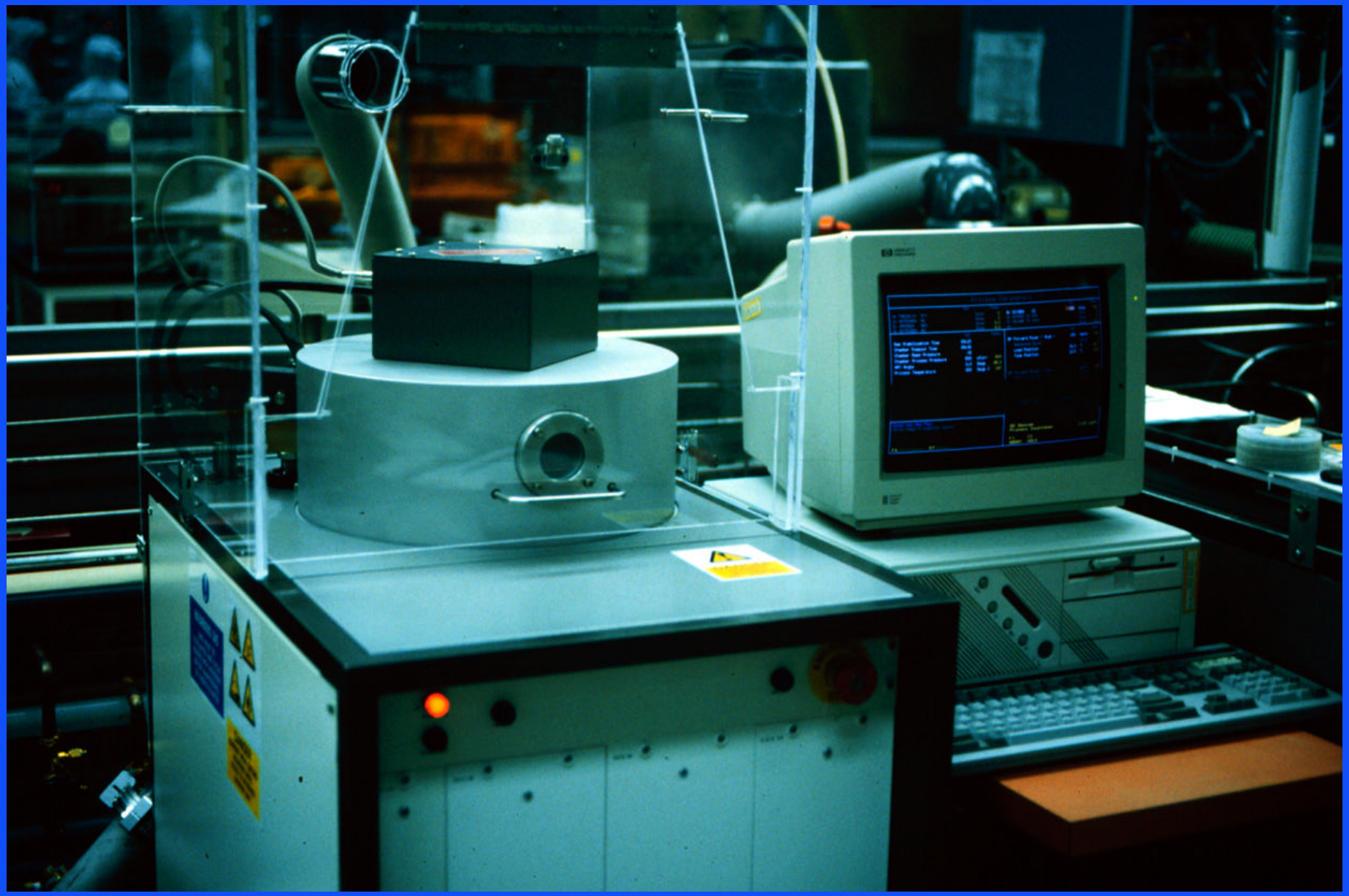
SILICON NITRIDE

- **Silicon nitride is an extremely useful dielectric material.**
- **Commonly deposited through LPCVD and PECVD.**
- **Can control stress with PECVD (13.56 MHz - Tensile, 50 kHz - Compressive, can mix them!).**
- **Some nitrides block alkali ions very well.**
- **Typical (PECVD) deposition reactions:**
  - **Silane and N_2O in Ar plasma: $SiH_4 + 4N_2O \rightarrow SiO_2 + 4N_2 + 2H_2O$**
  - **Silane in NH_3 in Ar plasma: $SiH_4 + NH3 \rightarrow SiNH + 3H_2$ ("theoretical" reaction: $3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$ at 700 to 900°C)**
  - **Silane in nitrogen plasma: $2SiH_4 + N_2 \rightarrow 2SiNH + 3H_2$**

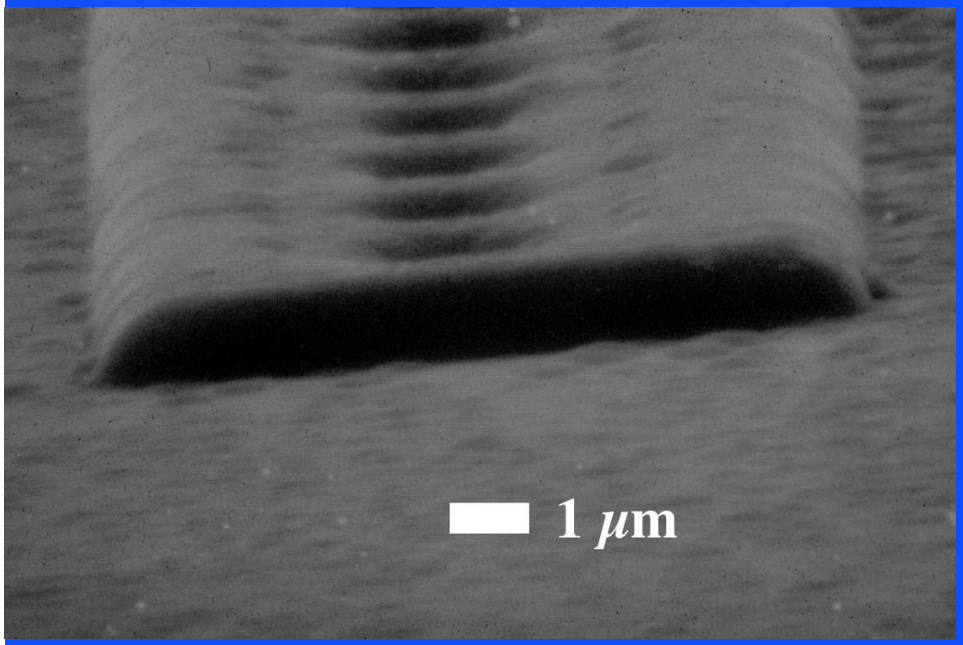
COMPARISON OF LPCVD & PECVD SILICON NITRIDES

Deposition Type	LPCVD	PECVD
Typical Temp.	700 to 800°C	< 250 to 350°C
Composition	$Si_3N_4(H)$	SiN_xH_y
Si/N Ratio	0.75	0.8 to 1.2
% H	4 to 8	20 to 25
Refractive Index	2.01	1.8 to 2.5
Density (g/cm^3)	2.9 to 3.1	2.4 to 2.8
Resistivity (Ω•cm)	10^{16}	10^6 to 10^{15}
Dielectric Strength (10^6 V/cm or 10^2 V/μm)	10	5
Energy gap (eV)	5	4 to 5
Stress (MPa)	1,000 tens (can be ≈ zero for Si rich films)	200 comp to 500 tens

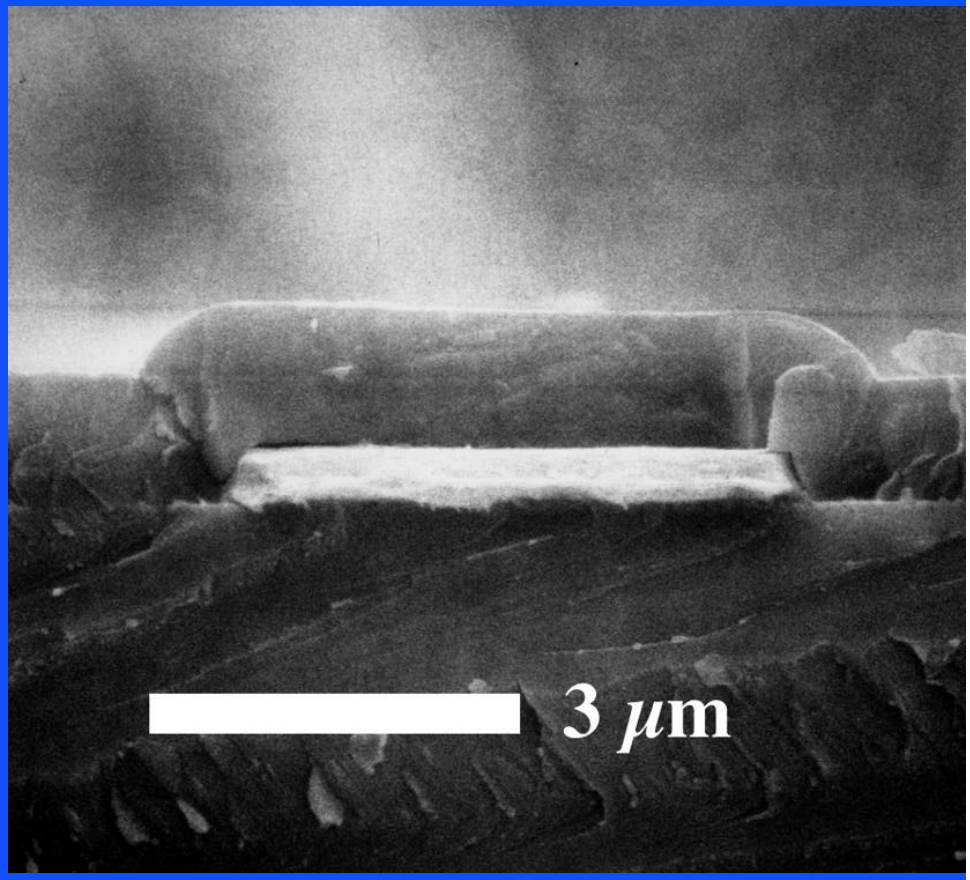
Reference: Adams (1983)...



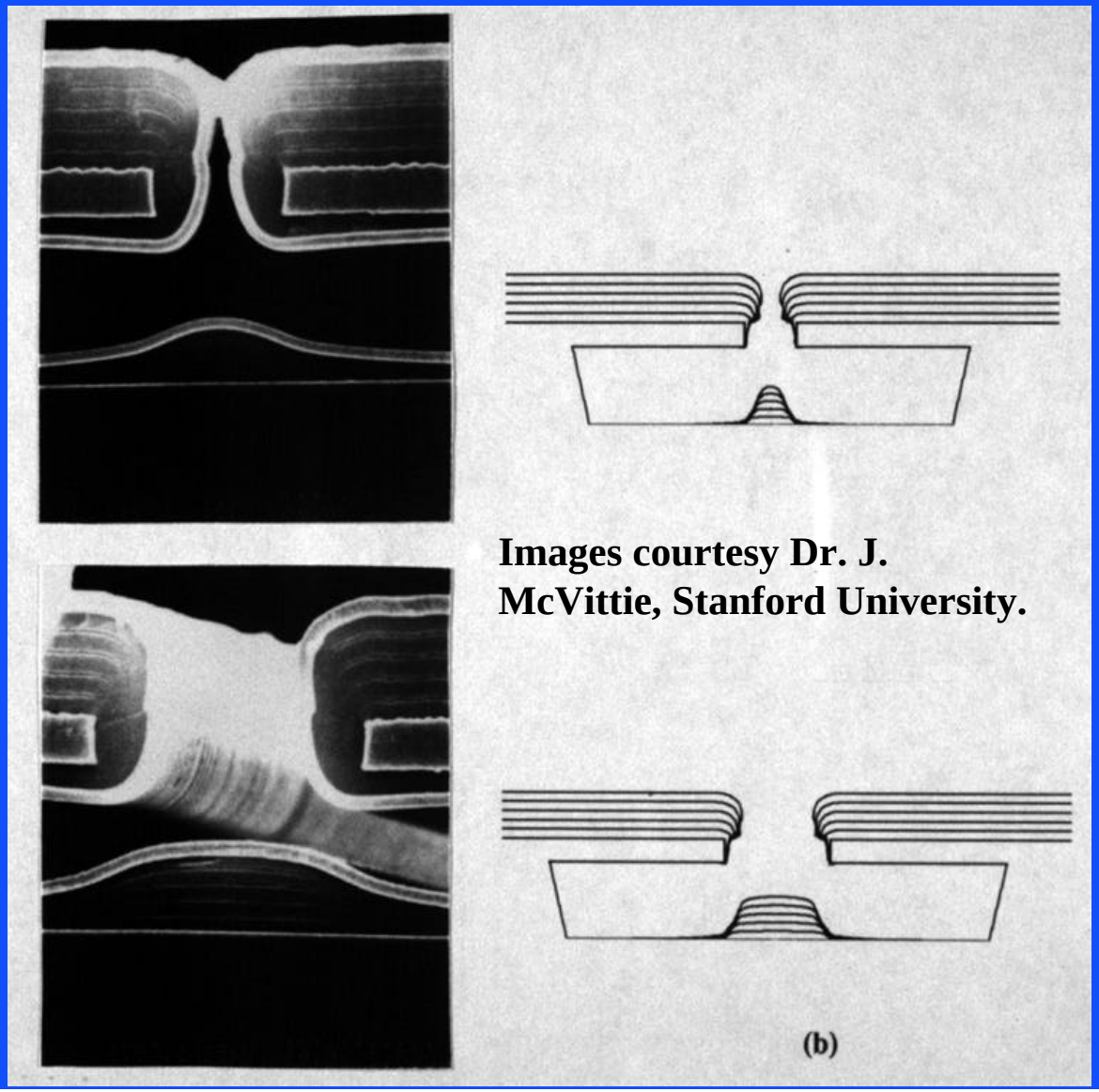
PECVD Silicon Nitride - Example of Conformal Coating Capability



PECVD silicon nitride on metal traces.



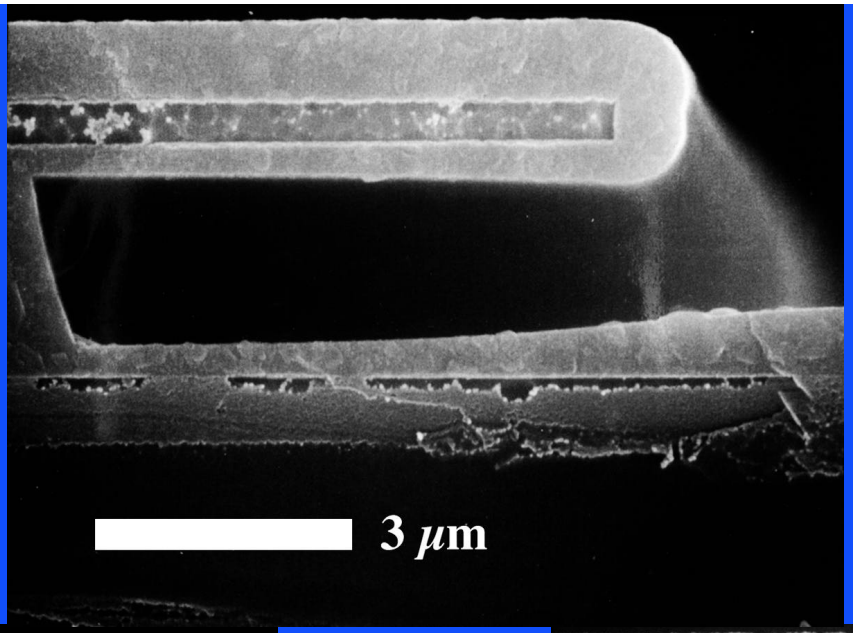
DEPOSITION TEST & MODELING

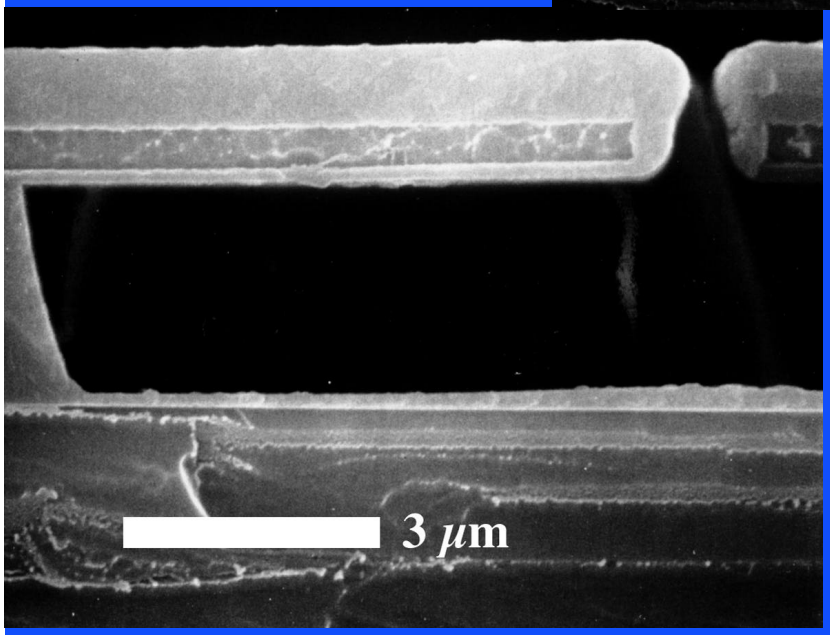


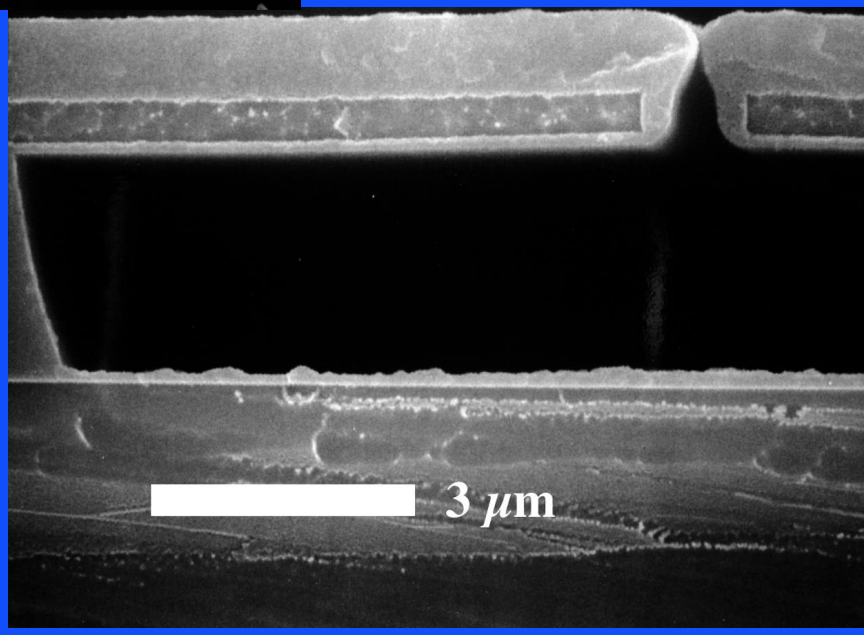
Images courtesy Dr. J. McVittie, Stanford University.

(b)

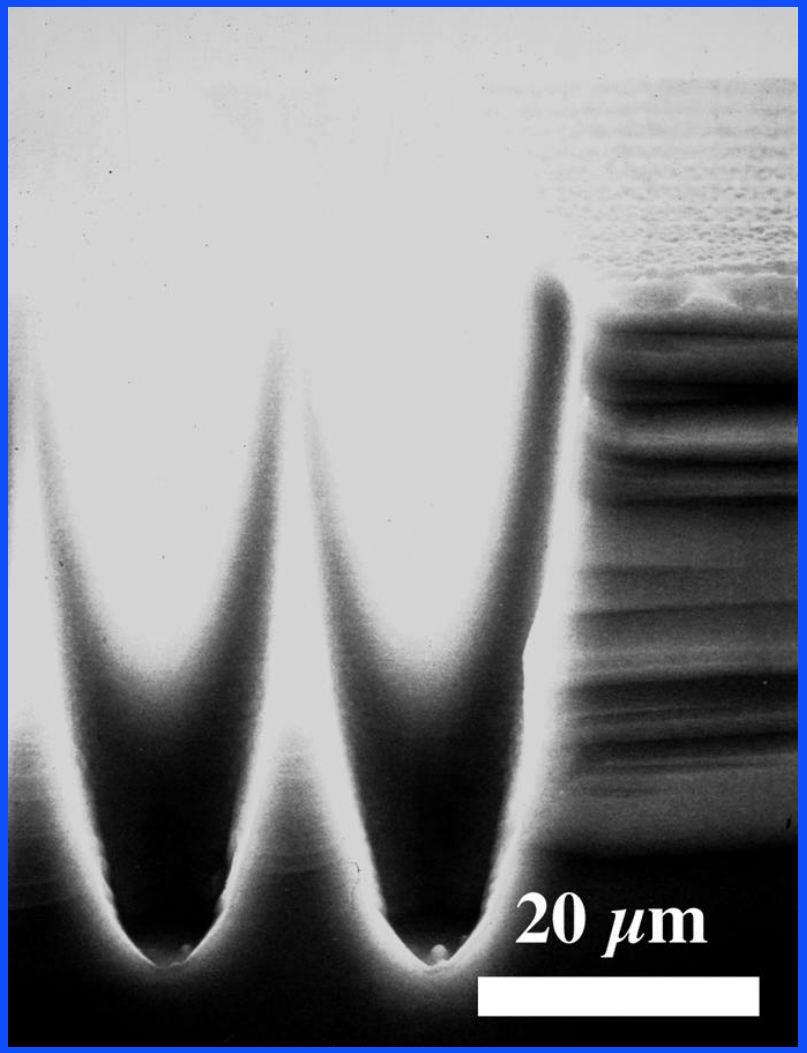
Images courtesy Dr. J. McVittie, Stanford University.

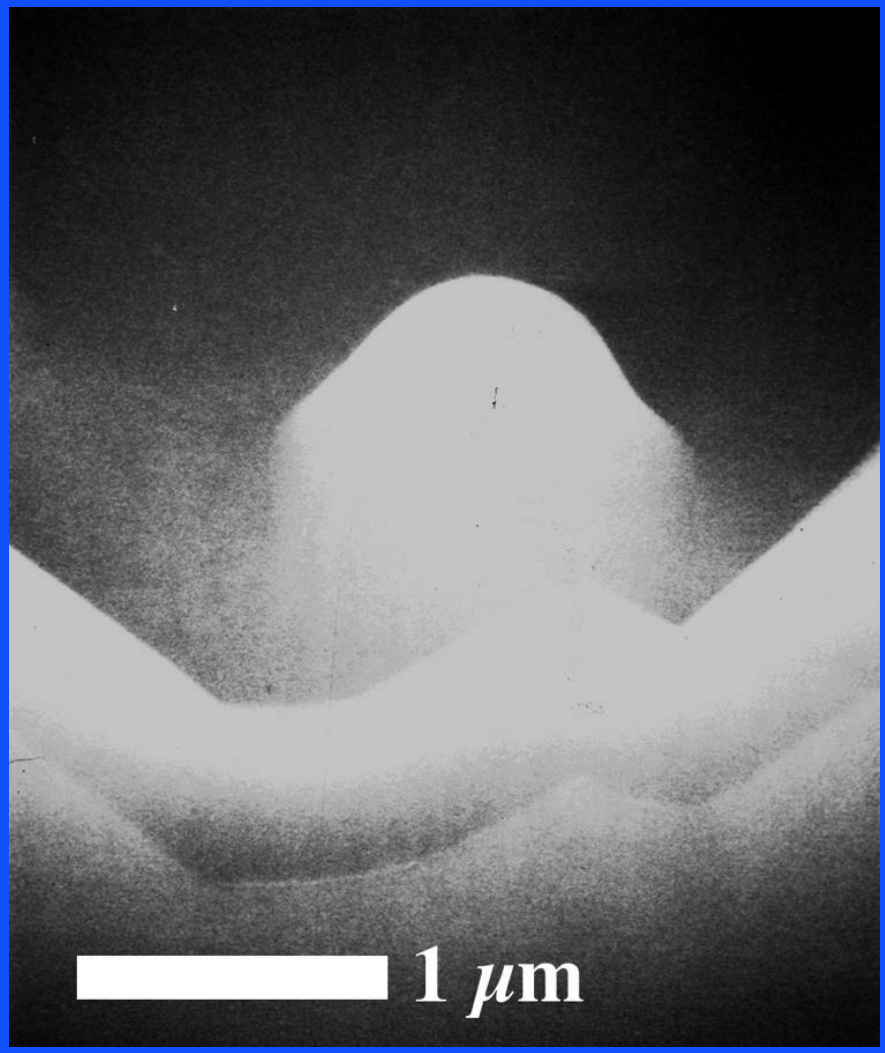






SILICON NITRIDE DEPOSITION TESTS





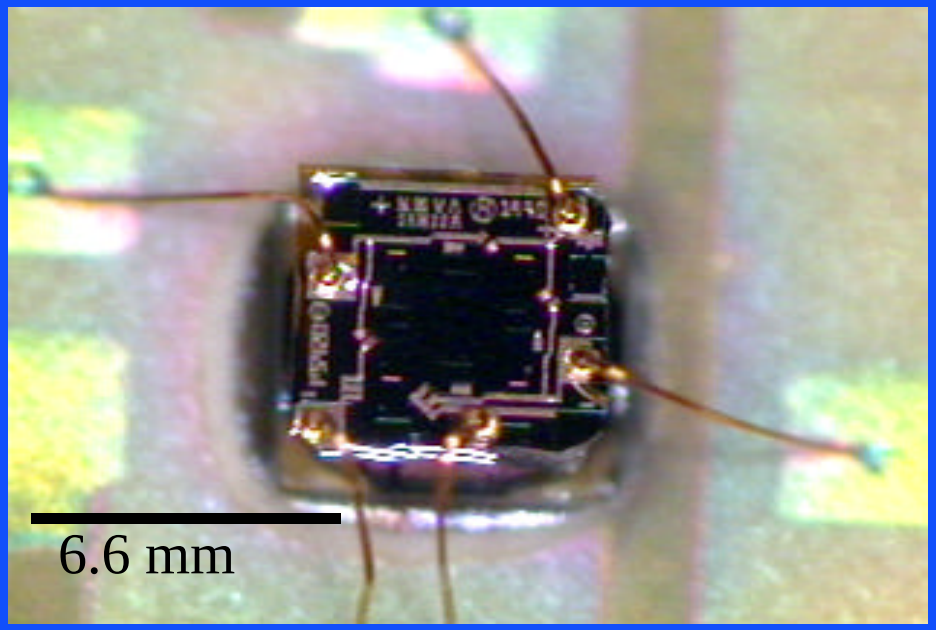
SILICON CARBIDE

- **Silicon carbide can readily be deposited using PECVD techniques, and is very useful due to its resistance to chemical attack and mechanical hardness.**
- **The reaction is:** $SiH_4 + CH_4 \rightarrow SiC + 4H_2$
- **As for other PECVD films, there can be considerable hydrogen incorporation.**
- **There is wide variation in the literature due to differing deposition techniques.**
- **When properly deposited, PECVD silicon carbide cannot be etched appreciably by any known wet etchant.**

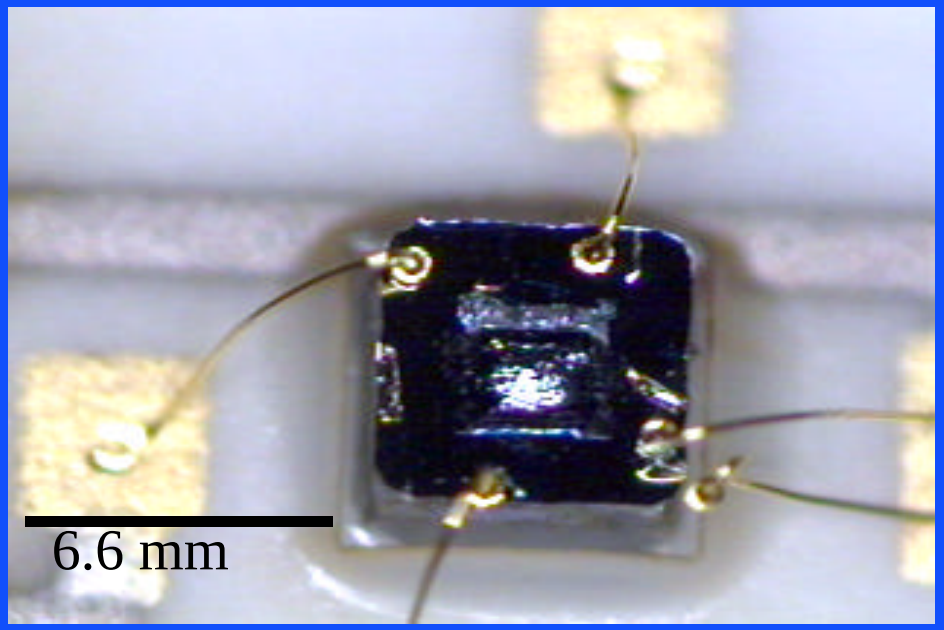
Flannery, A. F., Mourlas, N. J., Storment, C. W., Tsai, S., Tan, S. H., Heck, J., Monk, D., Gogoi, B., and Kovacs, G. T. A., "PECVD Silicon Carbide as a Chemically Resistant Material for Micromachined Transducers," Sensors and Actuators A, vol. 70, nos. 1 - 2, Oct. 1998, pp. 48 - 55.

WET ETCH RESISTANCE OF SILICON CARBIDE

Etch test of coated pressure sensor in 22% KOH at 80°C for 45 minutes.



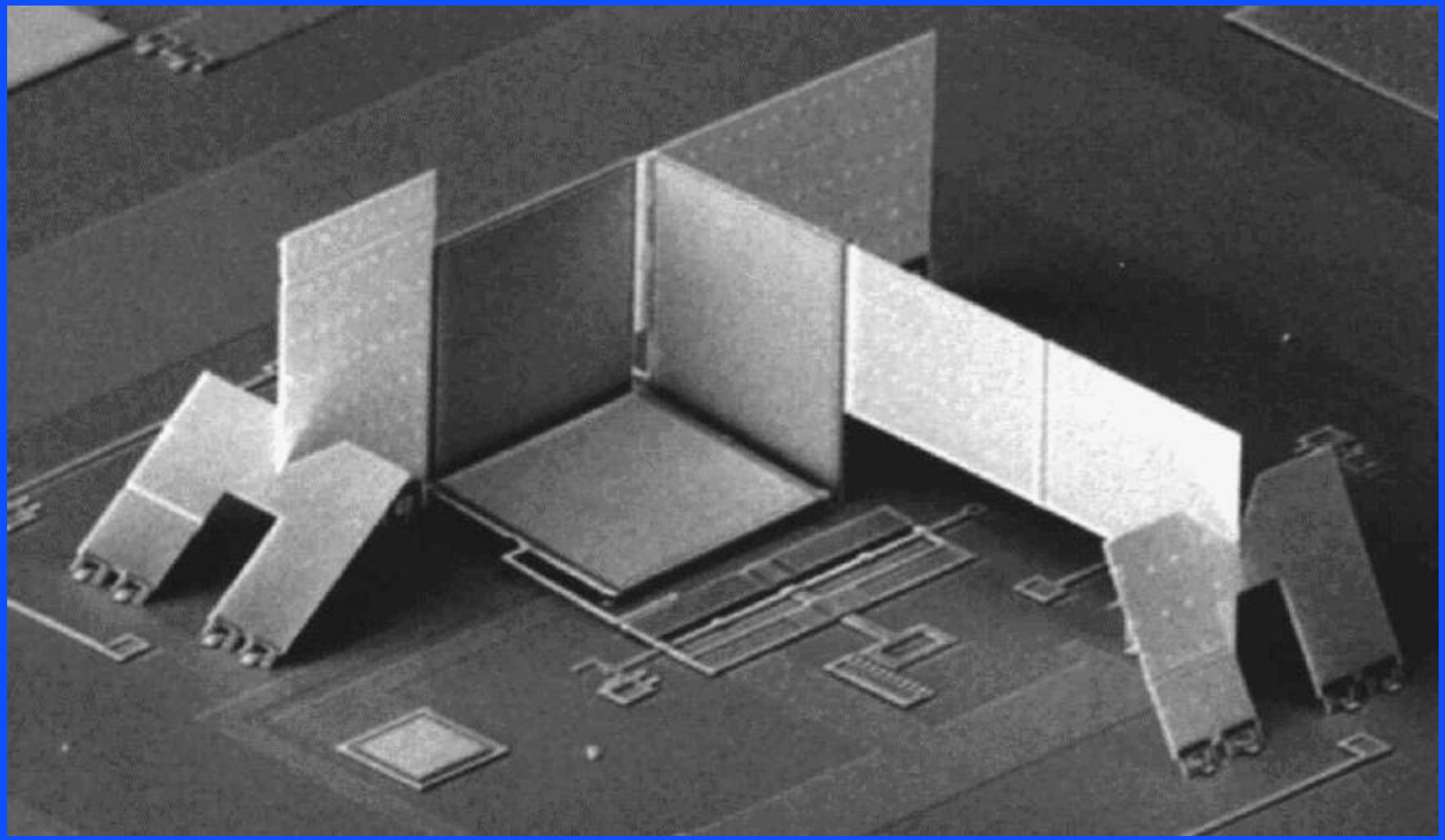
Coated with 300 nm PECVD SiC



Uncoated Pressure Sensor

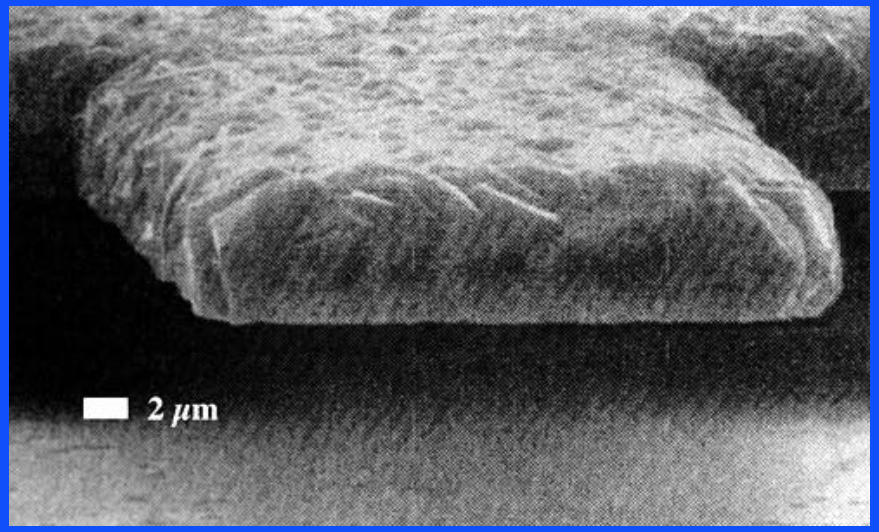
POLYSILICON

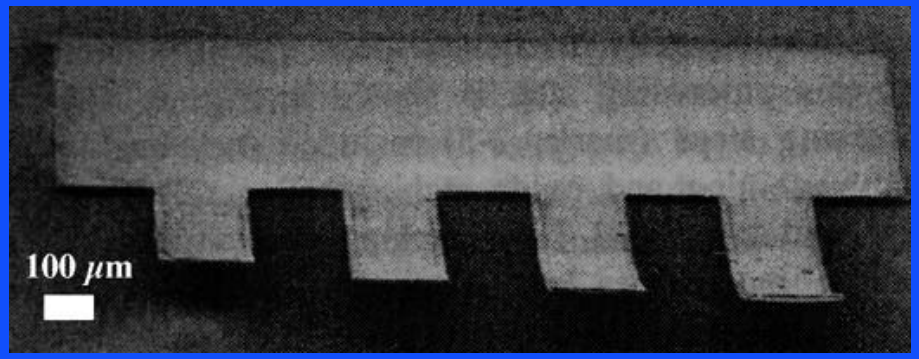
- **Polysilicon is readily available in MOS processes (for gates and interconnects) and is an important material in many surface micromachining processes.**
- **Polysilicon can be doped and used as a resistor or piezoresistor.**
- **Typically deposited through LPCVD by pyrolizing silane at 600 - 650°C (at lower temperatures, deposition rates too slow).**
- **The reaction is: SiH_4 –> Si + $2H_2$**
- **Fine structure strongly influenced by temperature, dopants, thermal history, etc.**
- **605°C = amorphous, 630°C = columnar**
- **PECVD is possible for deposition, but not commonly used.**



Courtesy E. Hui, U.C. Berkeley.

POLYCRYSTALLINE DIAMOND





Source: Aslam, Transducers '93

Aslam, M., and Schulz, D., "Technology of Diamond Microelectromechanical Systems," Proceedings of Transducers '95, the 8th International Conference on Solid-State Sensors and Actuators, Stockholm, Sweden, June 25 - 29, 1995, vol. 2, pp. 222 - 224.

SPUTTERED & SPIN-ON DIELECTRIC FILMS

- **Sputtered dielectrics are available, but RF sputtering is required.**
- **Spin-on glass is commonly used.**
- **Other spin-on dielectrics are available, but generally are not suitable for micromachining (yet?).**

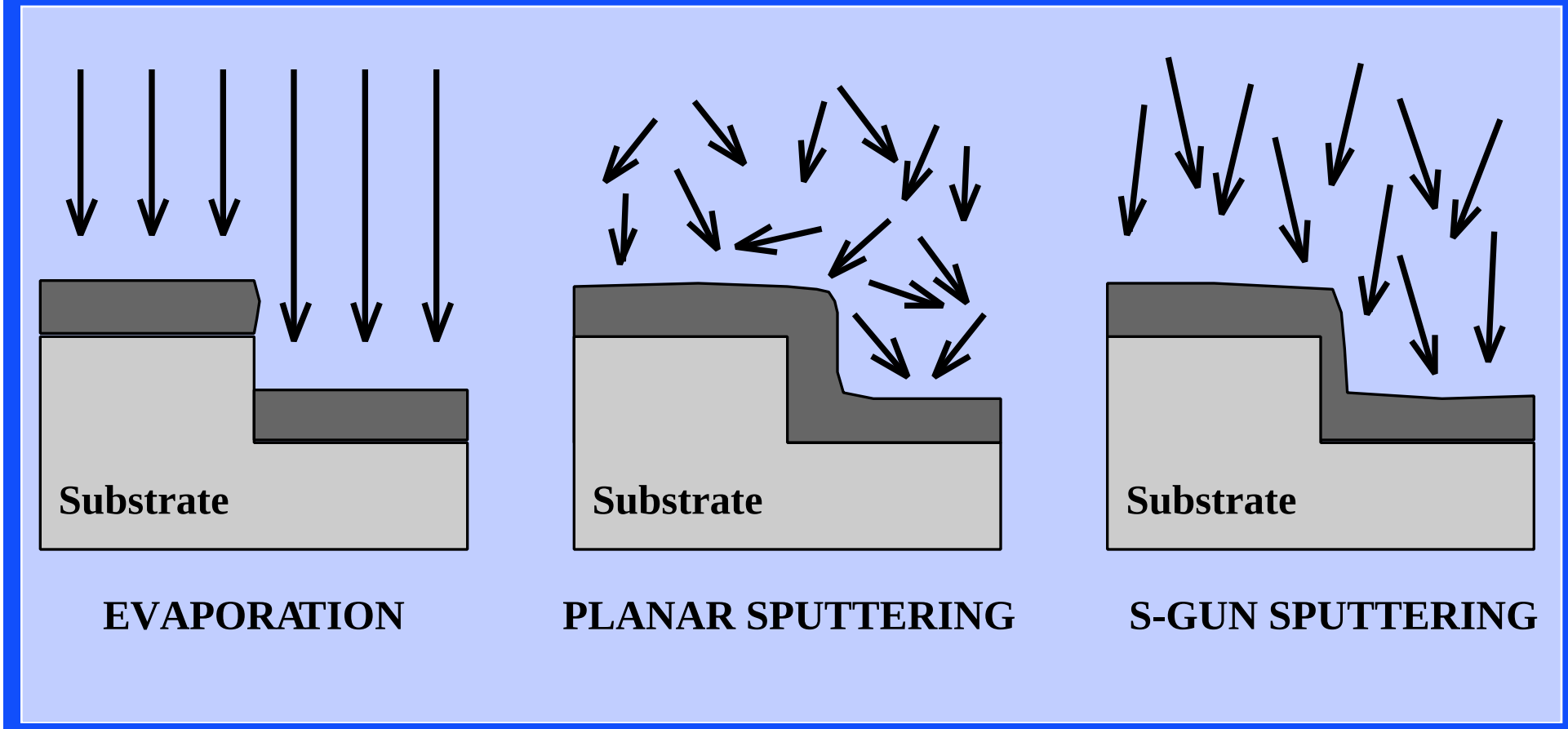
ETCHANTS FOR DIELECTRIC THIN FILMS

- **Dry etching is generally preferred if available.**
- **SiO_2 - HF, sometimes buffered with NH_3F, does not attack photoresist**
- **SiN_xH_y - hot H_3PO_4 (1 - 10 nm/min), can use SiO_2 masks (etched at ≈1/40th the rate)**
- **Polysilicon - same etchants as for single-crystal Si (KOH, TMAH, etc.), but etch rate may be higher.**
- **Organic films - H_2SO_4/H_2O_2 (Piranha) or O_2 plasma**

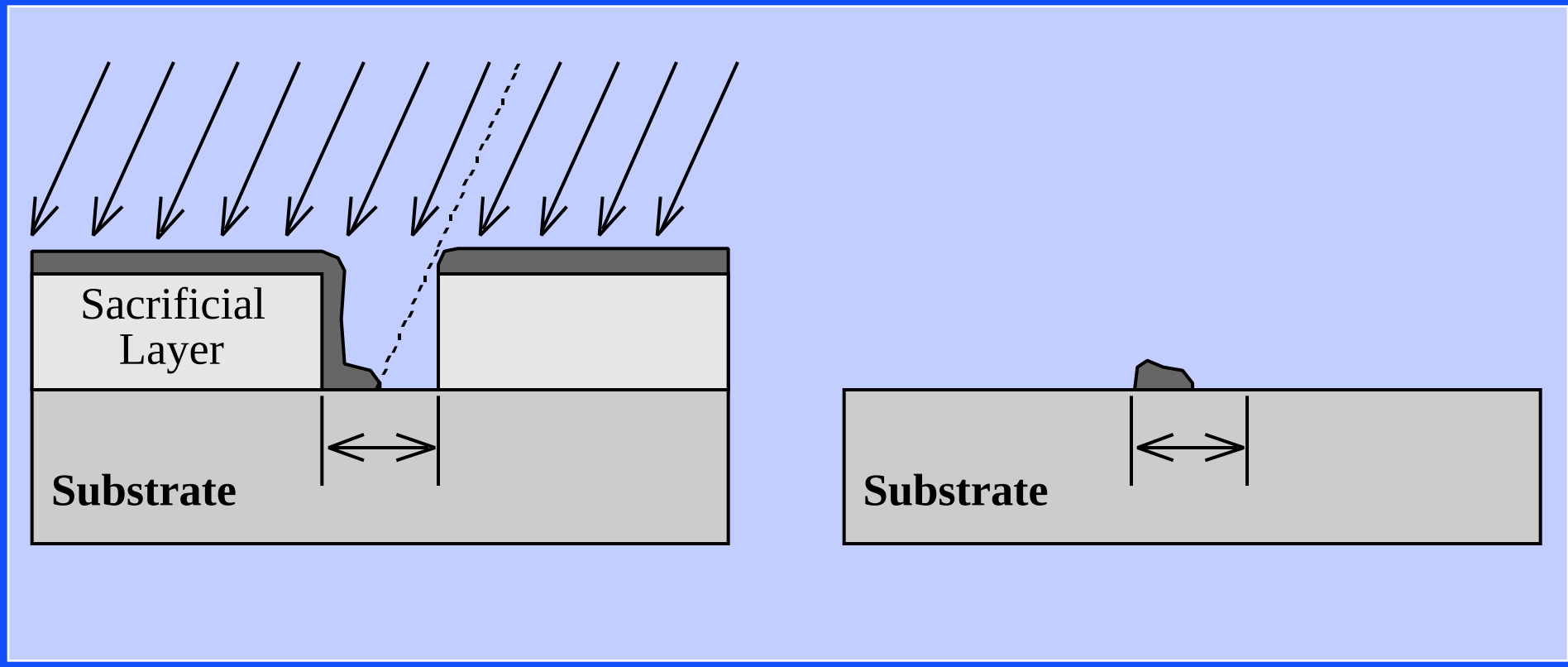
METALLIC THIN FILMS

- **Resistive evaporation uses an electrically heated wire or boat to evaporate the desired metal and may change composition of mixtures.**
- **Electron beams can also be used to evaporate metals.**
- **Evaporation is a condensation process, metal atoms "stick" as soon as they hit, resulting in poor step coverage (great for lift-off) and higher stress.**
- **Sputtering uses bombardment with inert ions (e.g. Ar^+) accelerated using DC or RF drive to mobilize metal and does not change mixture composition in most cases.**
- **More energy in metal atoms allows for more mobility (and re-sputtering) for better step coverage and stress control.**
- **Electron emission (2° from target) may significantly heat substrates.**
- **Magnetron sputtering uses permanent magnets to increase current density at target, lowering impedance and reducing 2° electron emissions.**

COMPARISON OF METAL DEPOSITION METHODS

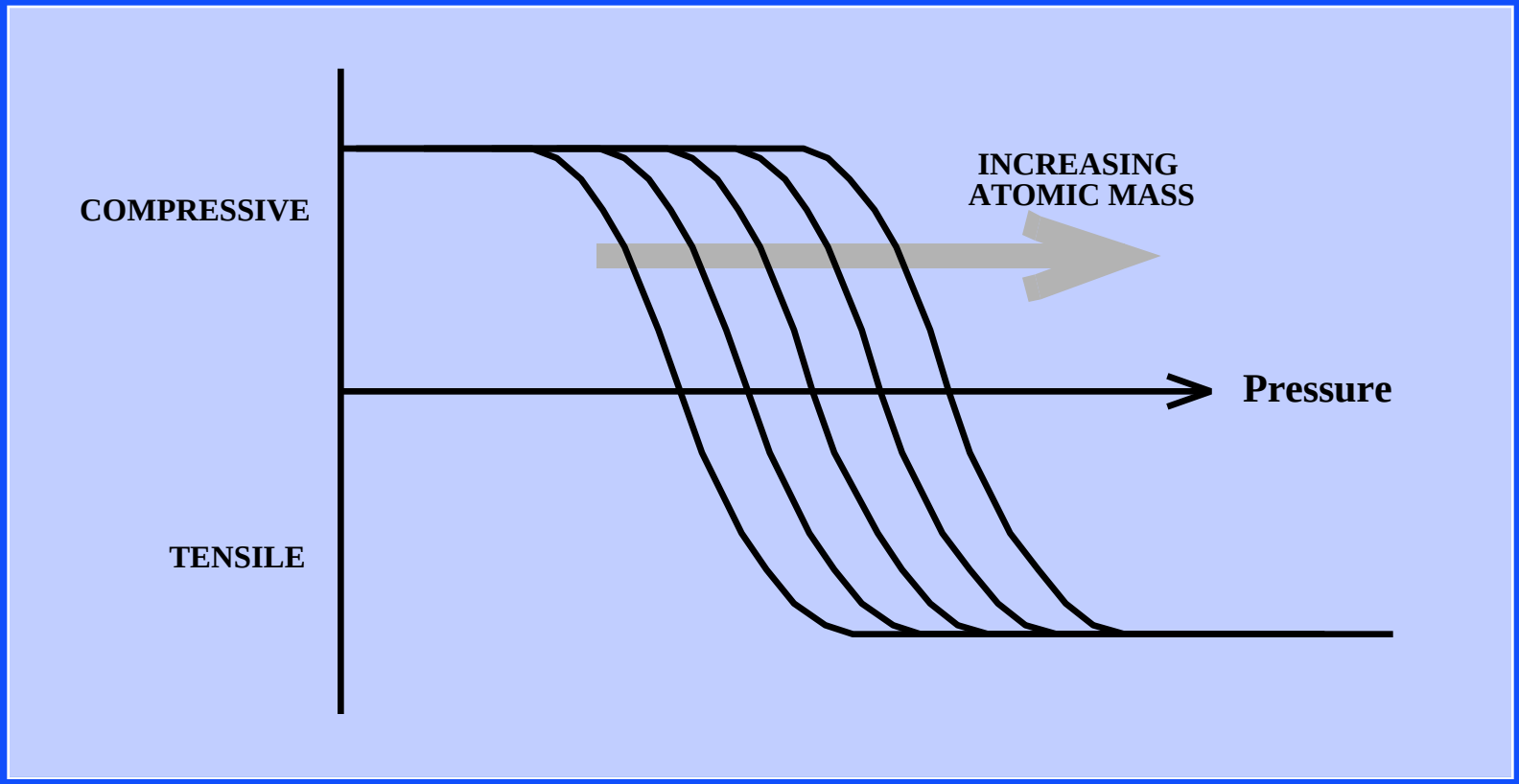


SHADOWING TO DECREASE FEATURE SIZE

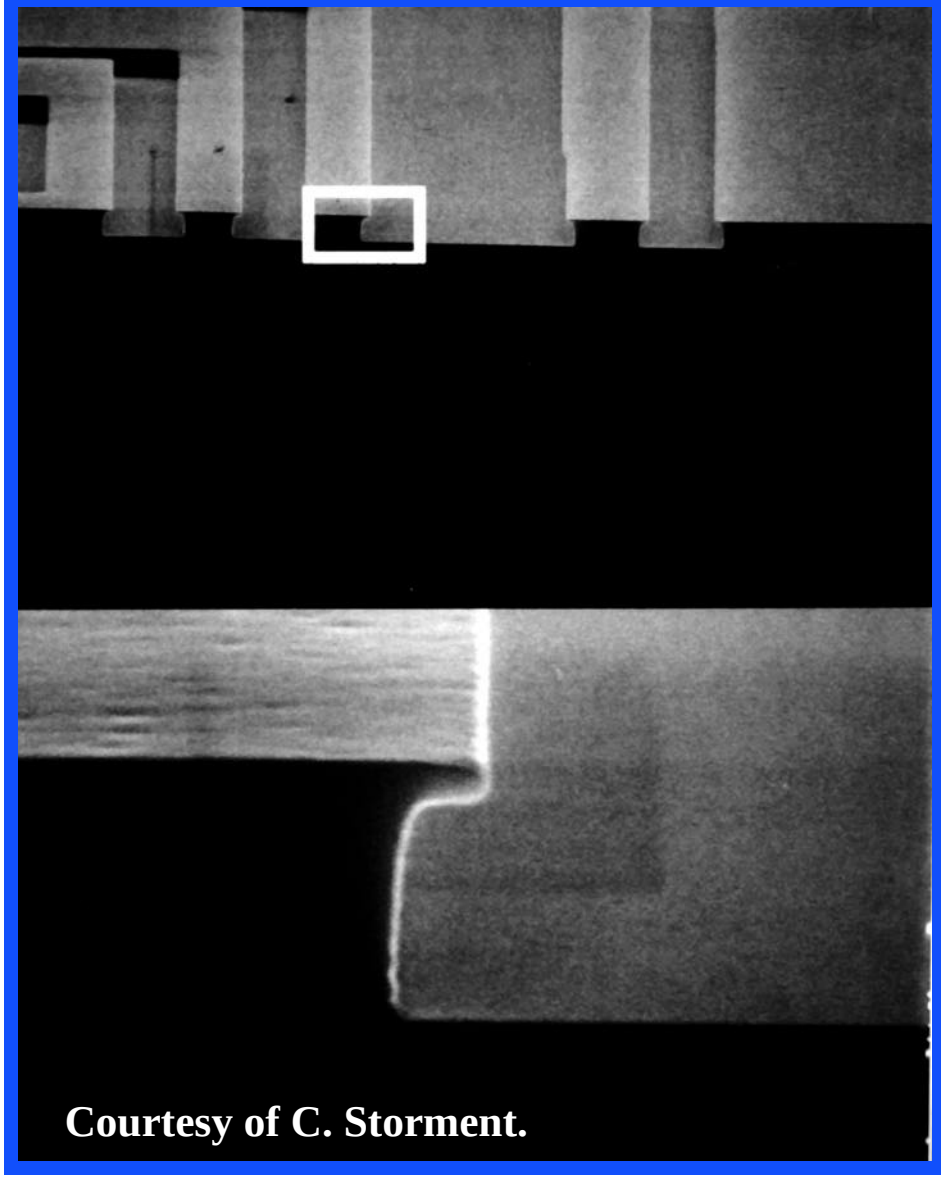


STRESSES IN SPUTTERED FILMS

- **Sputtered films are typically tensile, but stress can be controlled by working pressure for a given atomic mass.**

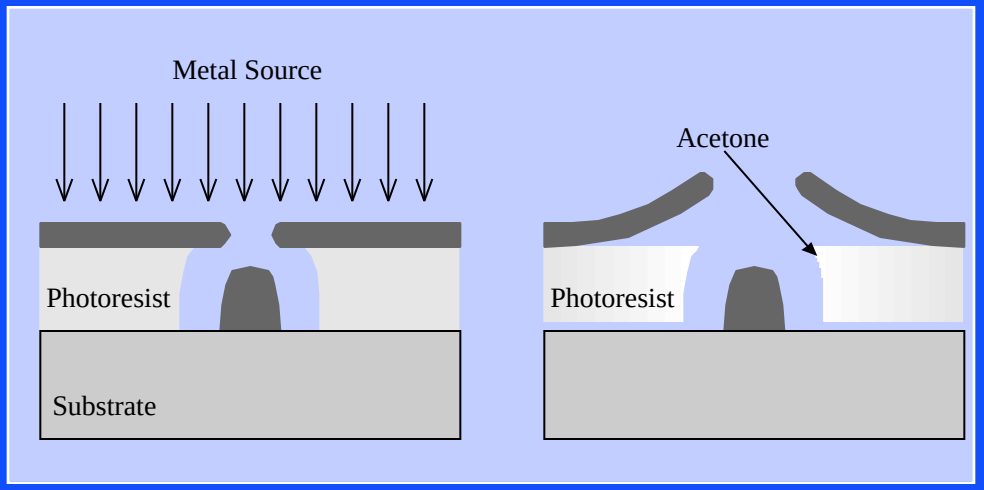


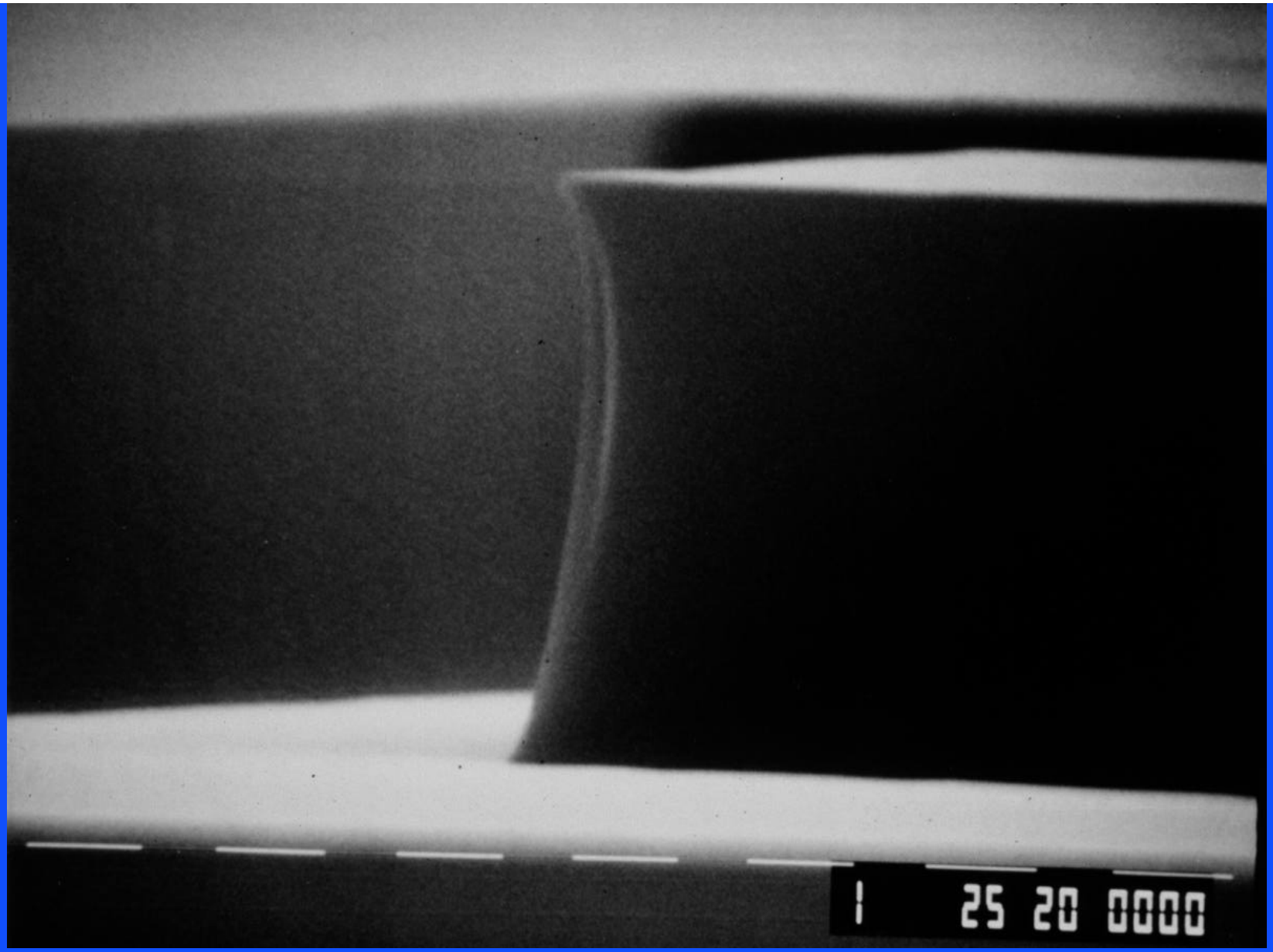
LIFT-OFF PATTERNING WITH PHOTORESIST



Courtesy of C. Storment.

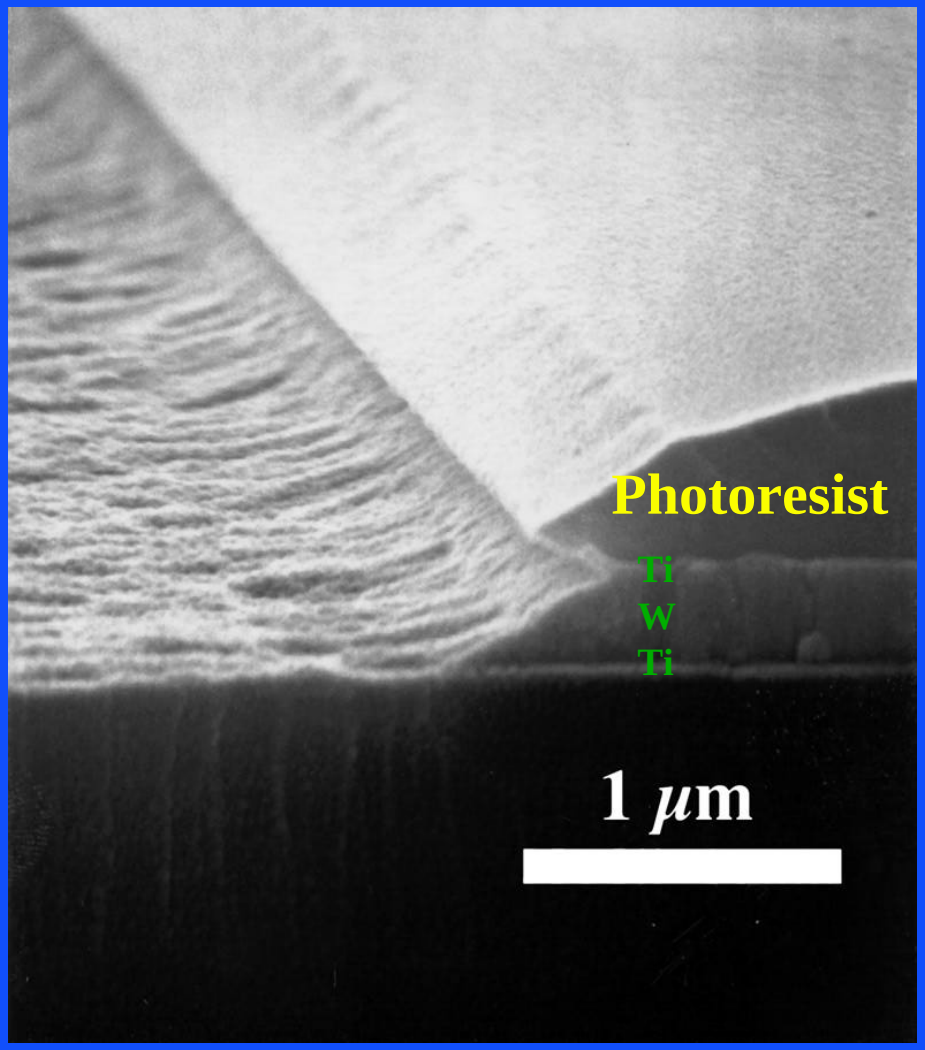
- **Photoresist-based lift-off involves a brief dip of exposed photoresist in chlorobenzene.**
- **The chlorobenzene penetrates only a slight distance, and slows down development of the resist in the thin top layer, forming the overhanging lip.**



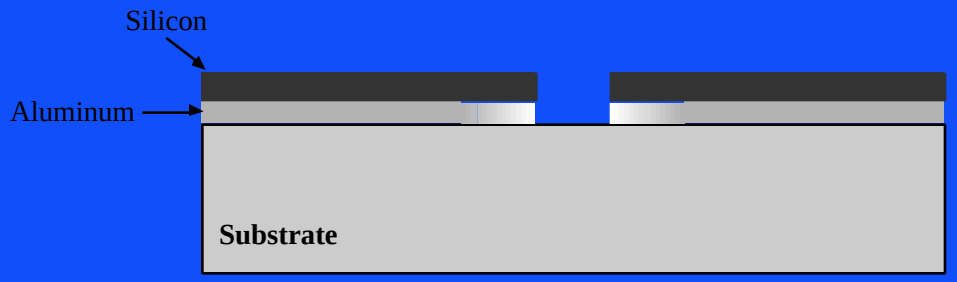


Courtesy of C. Storment.

MULTI-LAYER LIFT-OFF



- Many possible combinations of layers can be used to make lift-off structures where one layer is selectively undercut to form an overhang.
- Example: photoresist on top of a Ti/W/Ti trilayer, ten minute etch $SF_6 + C_2ClF_5$



ADHESION LAYERS

- Typically, thin layers (3 - 30 nm) of a reactive metal such as Ti, Hf, Cr, etc., is necessary for good adhesion of non-reactive metals such as Au, Pt, Ir, etc.
- Some of these metal combinations readily alloy (such as Ti/Au).
- One can selectively remove (or not deposit) the adhesion layer to allow regions to peel away.

METALS BY CVD AND SELECTIVE CVD

- CVD of metals from volatile organometallic and other compounds is possible for W, Mo, Ta, Ti (also Al in research).
- Selective metal CVD replaces silicon atoms with metal, so masked silicon shows no deposition.
- Typical reaction: $2WF_6 + 3Si \rightarrow 2W + 3SiF_4$

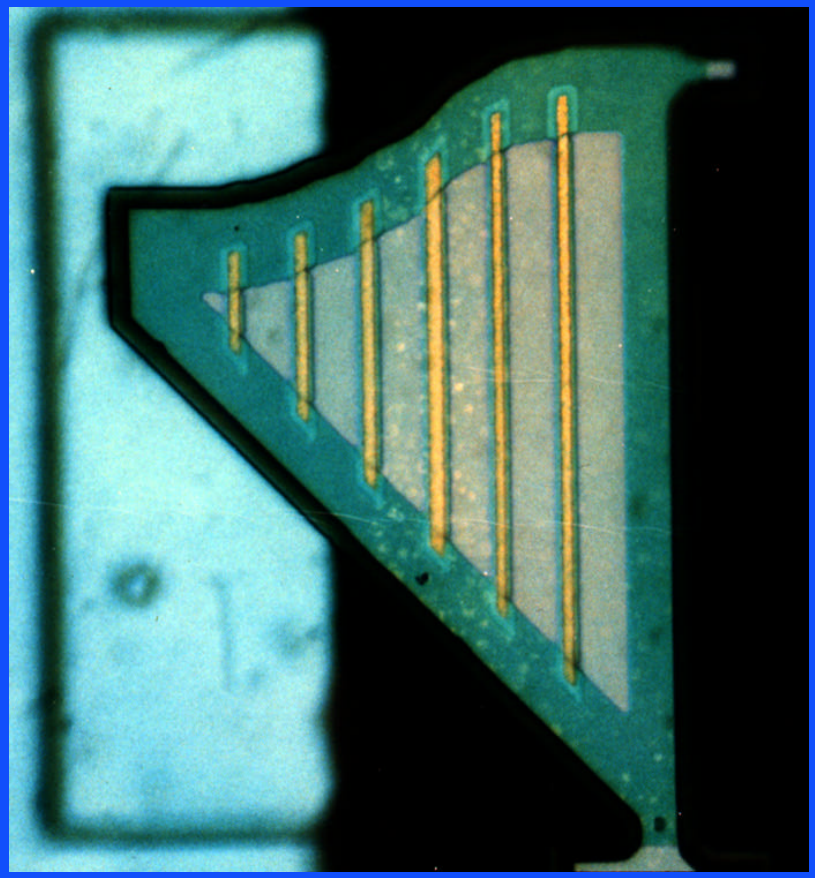
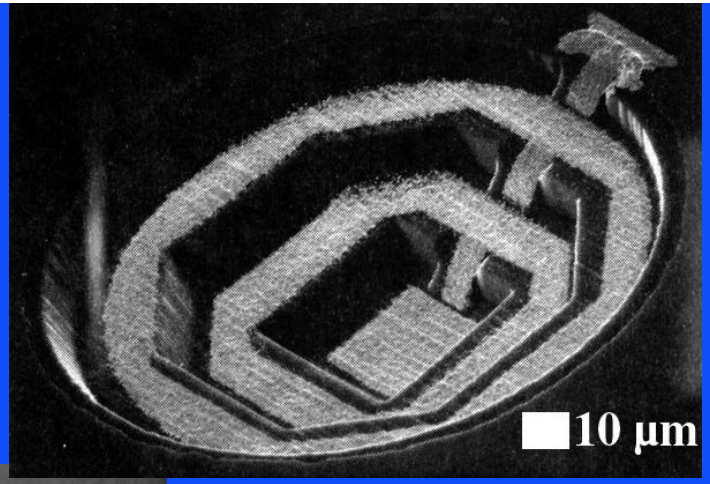


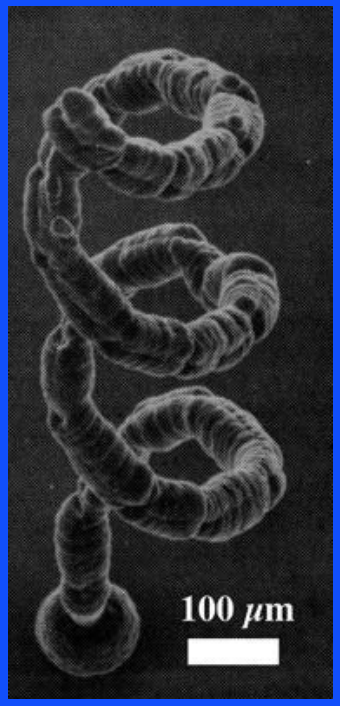
Image of CVD W "strings" on micro harp (≈ 100 µm) courtesy Dr. H. Busta.

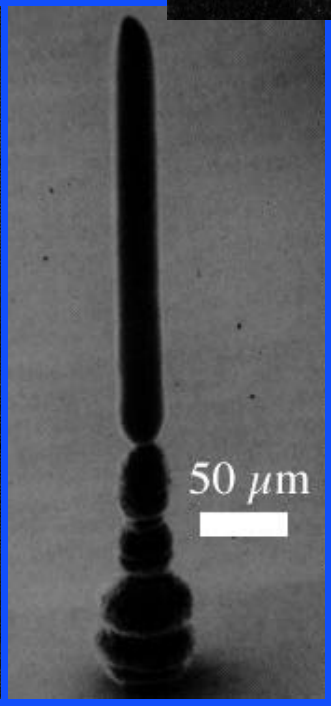
Busta, H. H., Feinerman, A. D., Ketterson, J. B., and Cueller, R. D., "Strings, Loops and Pyramids - Building Blocks for Microstructures," 1987 IEEE Micro Robots and Teleoperators Workshop, Hyannis, MA, Nov. 1987, pp. 9/1 - 9/5.

LASER-DRIVEN DEPOSITION

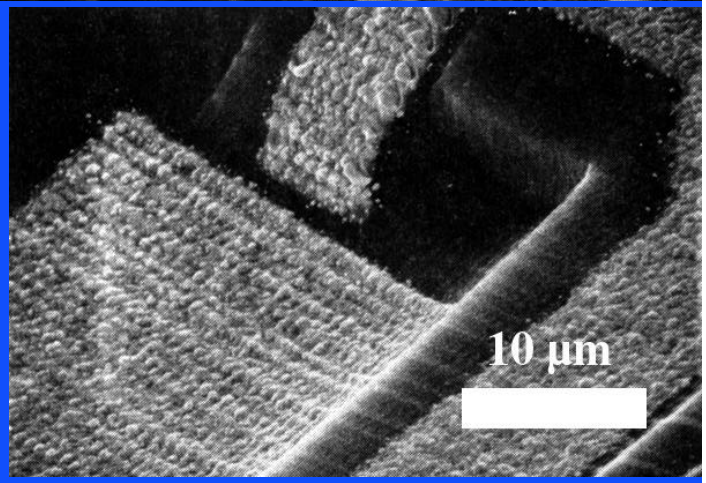
- **Lasers can be used to supply thermal energy to drive a metal deposition reaction.**
- **Pt can be deposited from $Pt(PF_3)_4$, Cobalt from $Co_2(CO)_{10}$, and W from WF_6/H_2**
- **Complex 3-D structures can be (serially) fabricated.**
- **Boron can also be deposited from BCl_3, and silicon from SiH_4, both in amorphous or polycrystalline forms, depending upon laser energy.**







Source: Westberg, H., Boman, M., Johansson, S., and Schweitz, J.-Å., "Truly Three Dimensional Structures Microfabricated by Laser Chemical Processing," Proceedings of Transducers '91, the 1991 International Conference on Solid-State Sensors and Actuators Digest of Technical Papers, IEEE Press, San Francisco, CA, June 24 - 27, 1991, pp. 516-519.

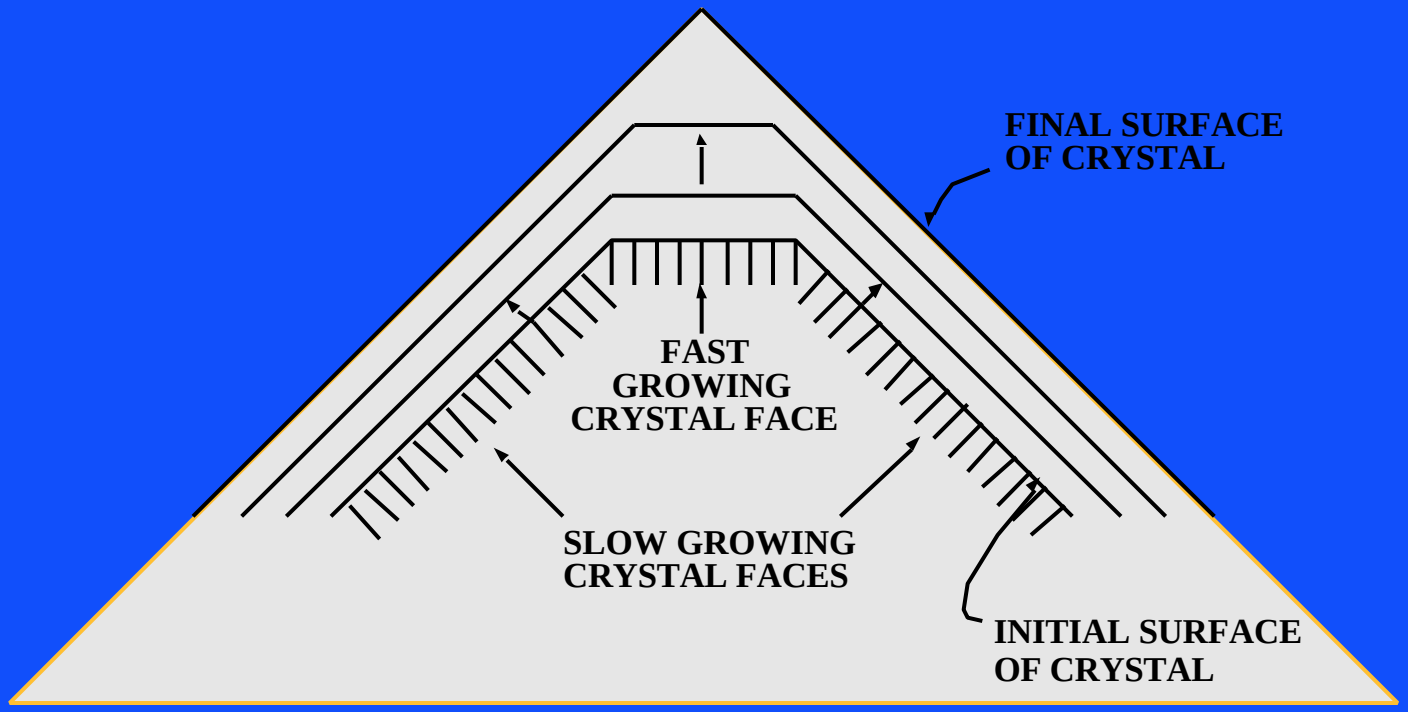


Source: Bloomstein, T. M., and Ehrlich, D. J., "Laser Deposition and Etching of Three-Dimensional Microstructures," Proceedings of Transducers '91, the 1991 International Conference on Solid-State Sensors and Actuators Digest of Technical Papers, IEEE Press, San Francisco, CA, June 24 - 27, 1991, pp. 507 - 511.

PLATING

- **Plating processes use the reduction of metal ion species in solution (generally aqueous) to form solid metal.**
- **Many metals and alloys can be plated (e.g. Au, Ag, Cu, Hg, Ni, Pt, Permalloy [NiFe], etc.).**
- **Electroless plating uses reducing agents to drive metal deposition.**
- **Electroplating uses electrical current to drive the reduction.**
- **Pulsing the electroplating current allows time between pulses for diffusion to replenish reactants (stress control, control over morphology, etc., possible).**
- **Under diffusion-limited conditions, amorphous (“black”) metal layers can be plated (very high surface areas).**

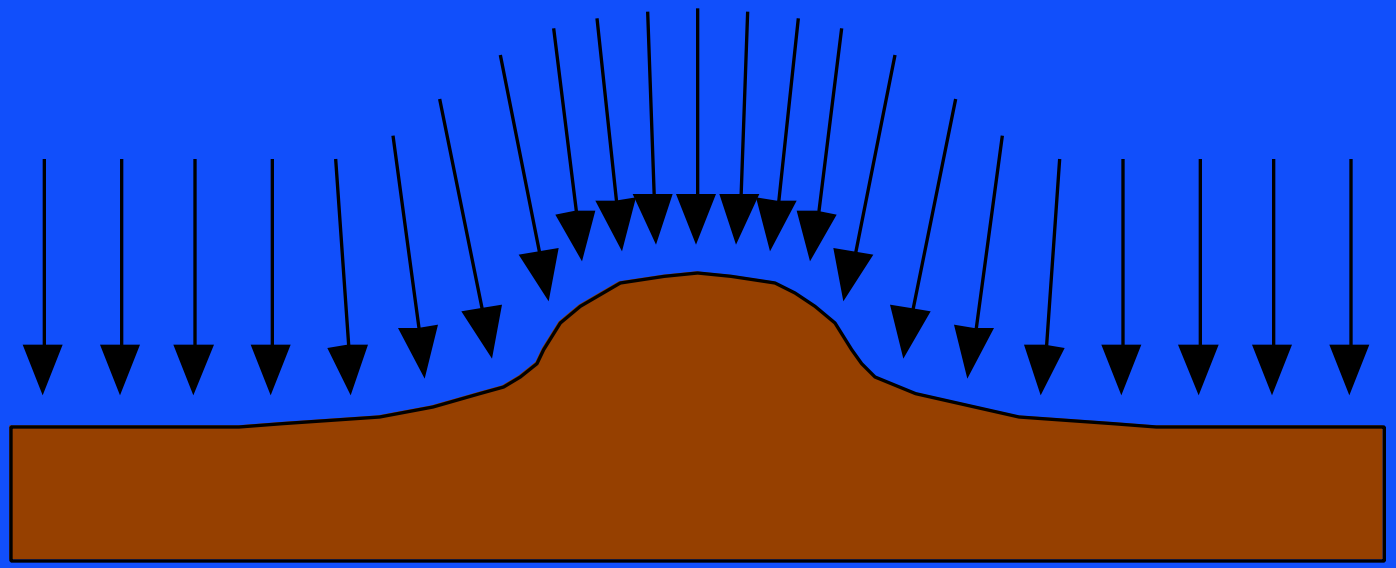
FAST-GROWING CRYSTAL FACES DISAPPEAR IN ELECTROPLATING



After Bockris and Reddy (1970).

Bockris, J. O'M., and Reddy, K. N., "The Electrogrowth of Metals on Electrodes," Section 10.2 in "Modern Electrochemistry," Plenum Press, New York, NY, 1970, pp. 1173 - 1231.

PREFERENTIAL PLATING AT HIGH-FIELD POINTS

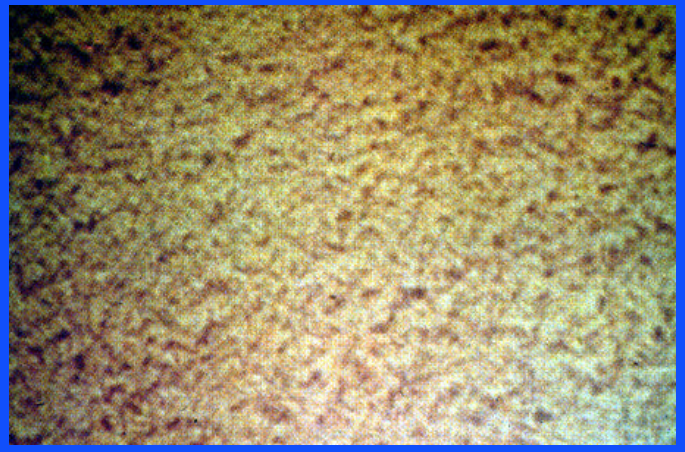


After Bockris and Reddy (1970).

Bockris, J. O'M., and Reddy, K. N., "The Electrogrowth of Metals on Electrodes," Section 10.2 in "Modern Electrochemistry," Plenum Press, New York, NY, 1970, pp. 1173 - 1231.

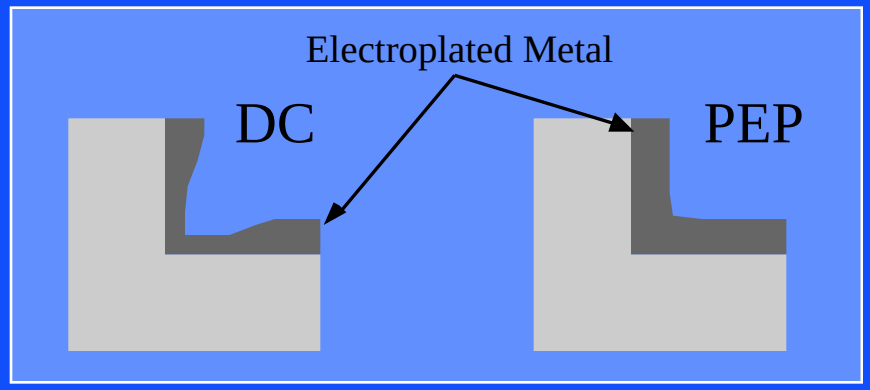
PULSED VERSUS DC ELECTROPLATING

DC plated Au, 3A/ft^2, 5 µm.



Pulse plated Au, 3A/ft^2, 5 µm.

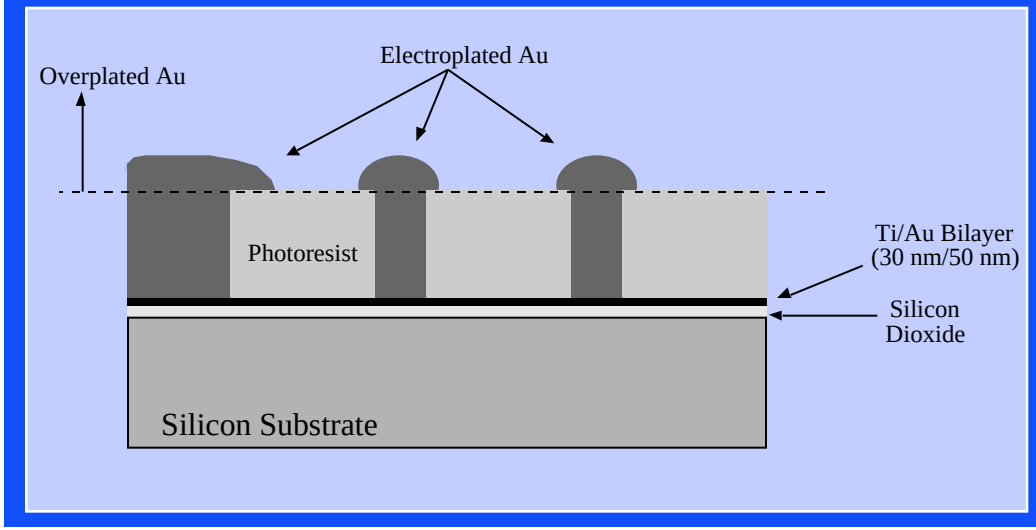
- Pulsed application of current in electroplating can result in finer grains, stress control (via duty cycle), some control over crystal orientation, and better deposition in corners ("throwing power").
- Down-sides include increased contaminants and potentially less uniform current distributions.

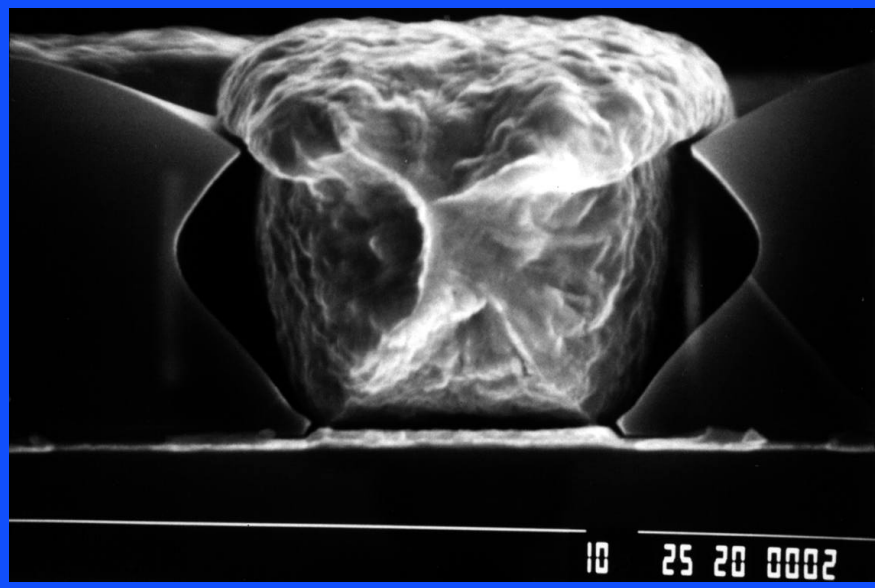


TEMPLATE-BASED PLATING

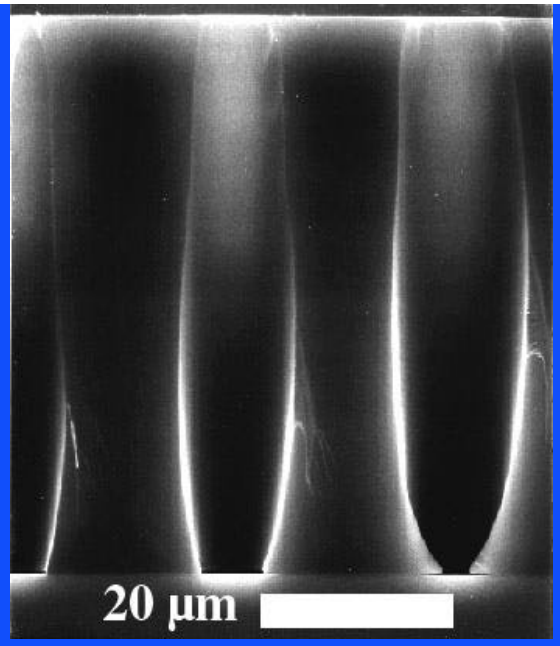
- **Template methods, often using organic materials such as photoresist, can be used to define where plating takes place.**
- **Multi-level templates are possible.**

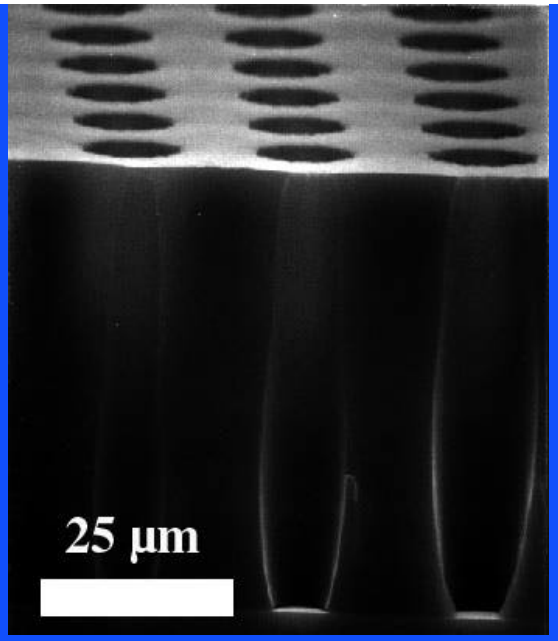
SEMs courtesy of C. Storment.

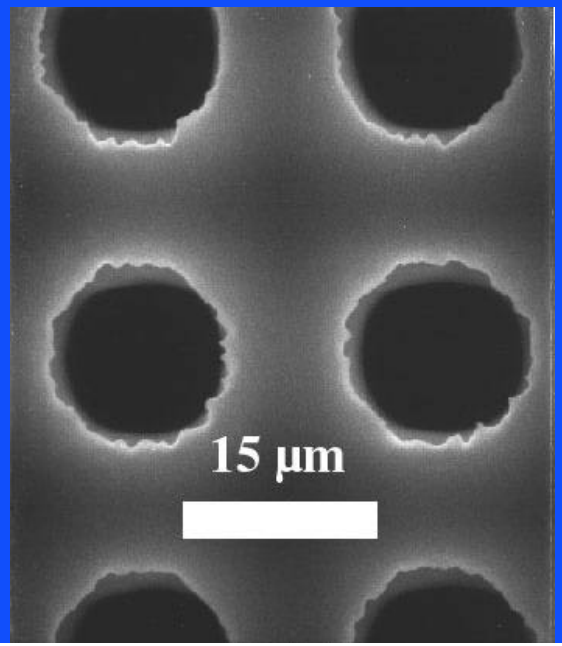


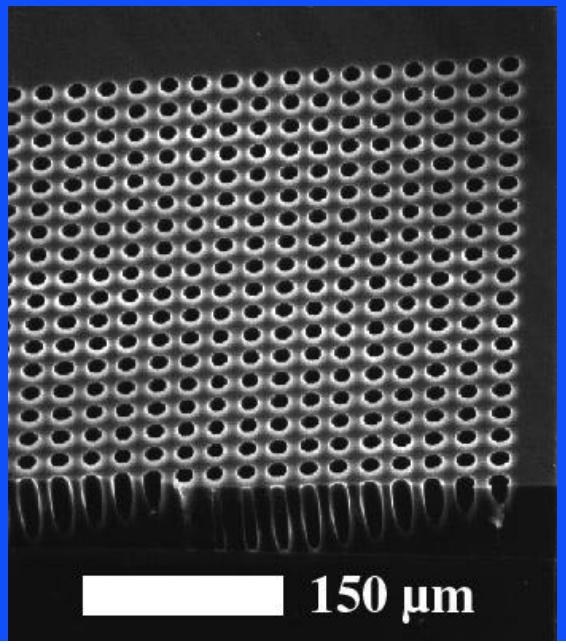


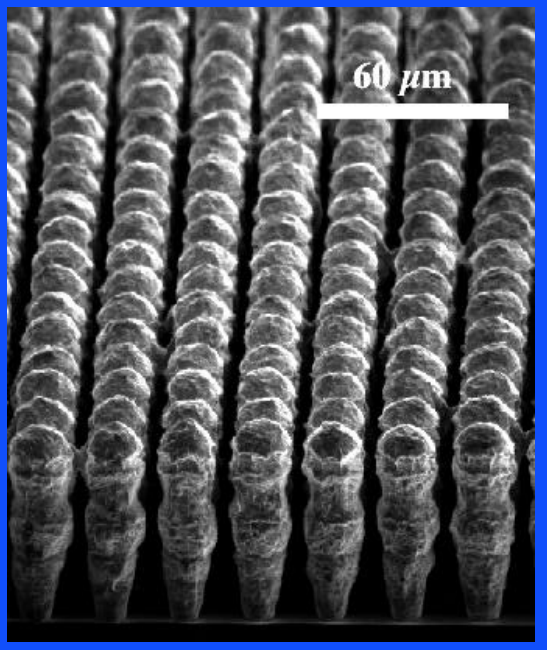
PHOTORESIST TEMPLATE



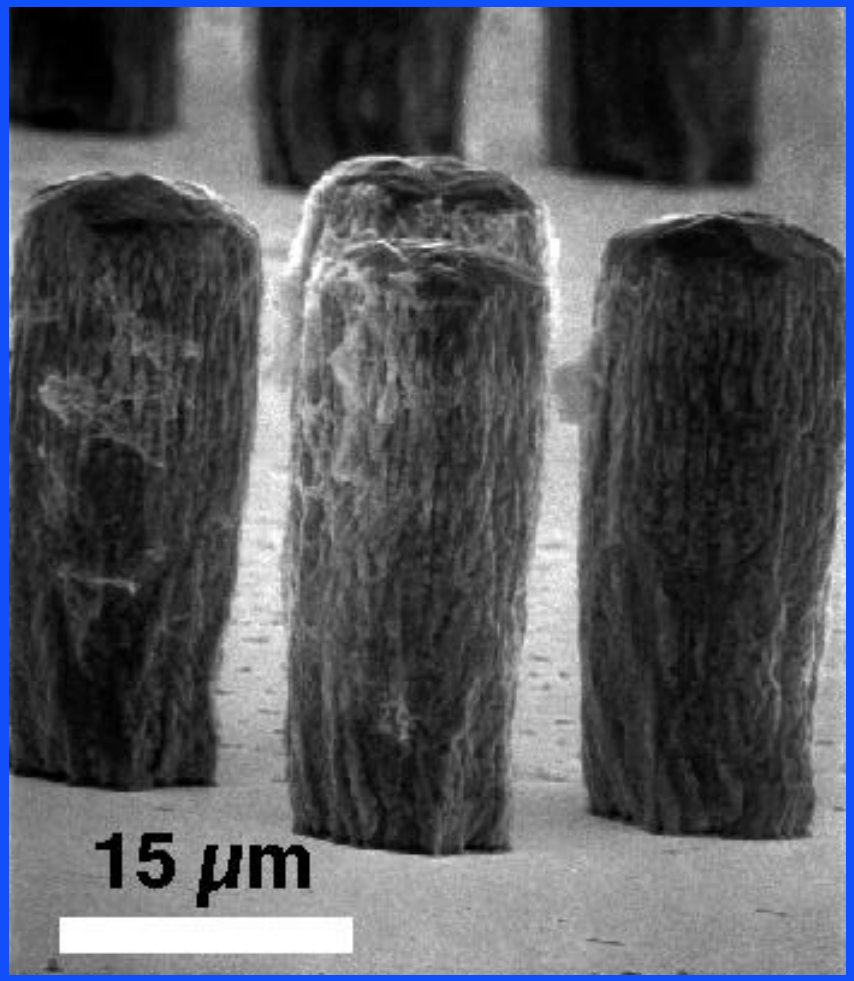


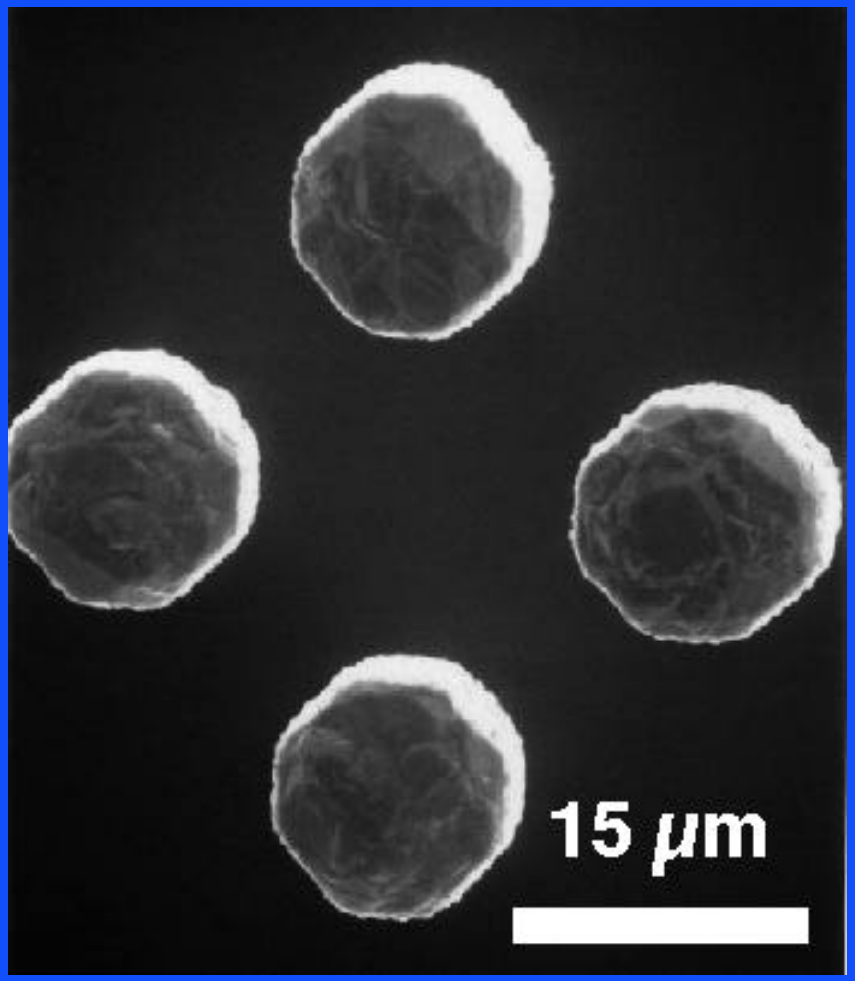




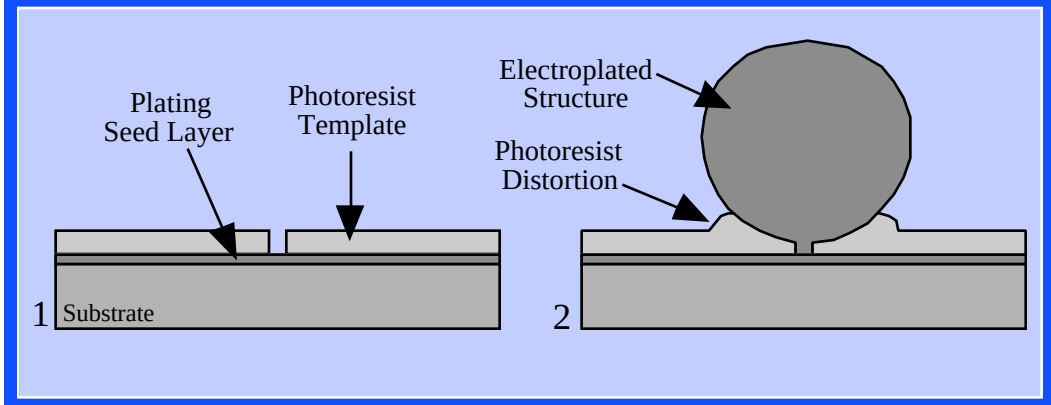


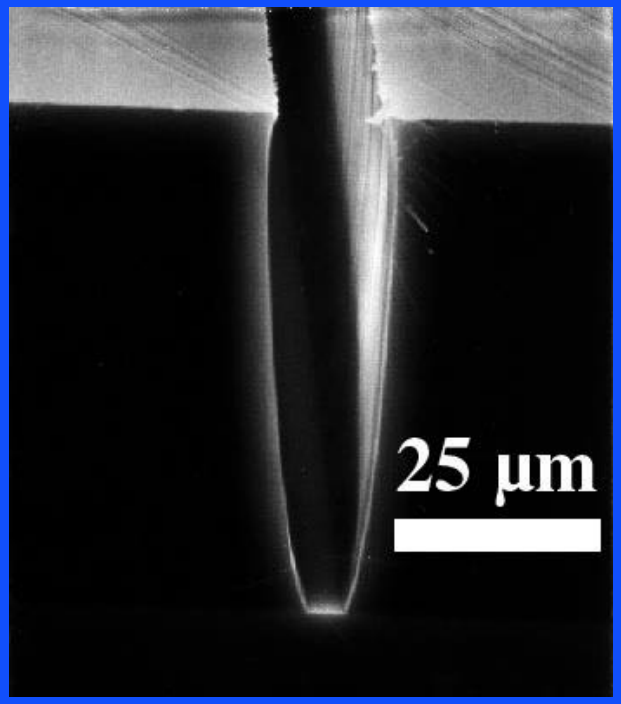
POLYIMIDE TEMPLATE (OXYGEN RIE ETCHED)

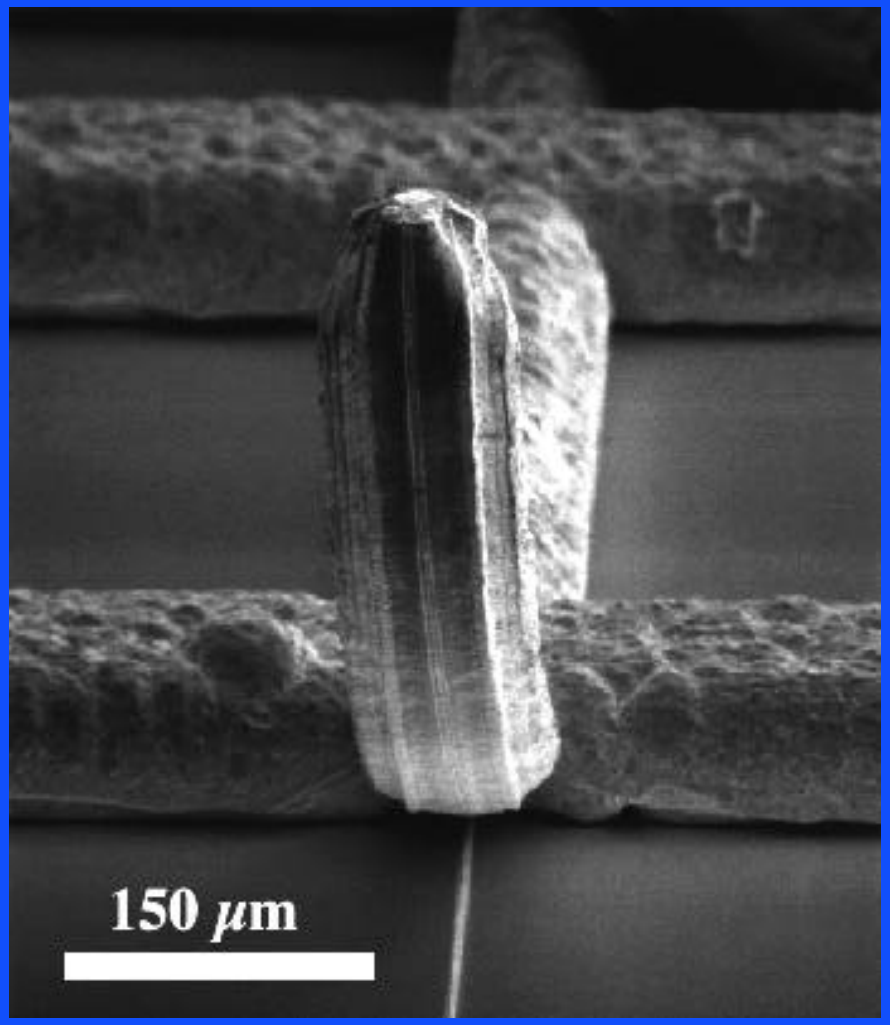


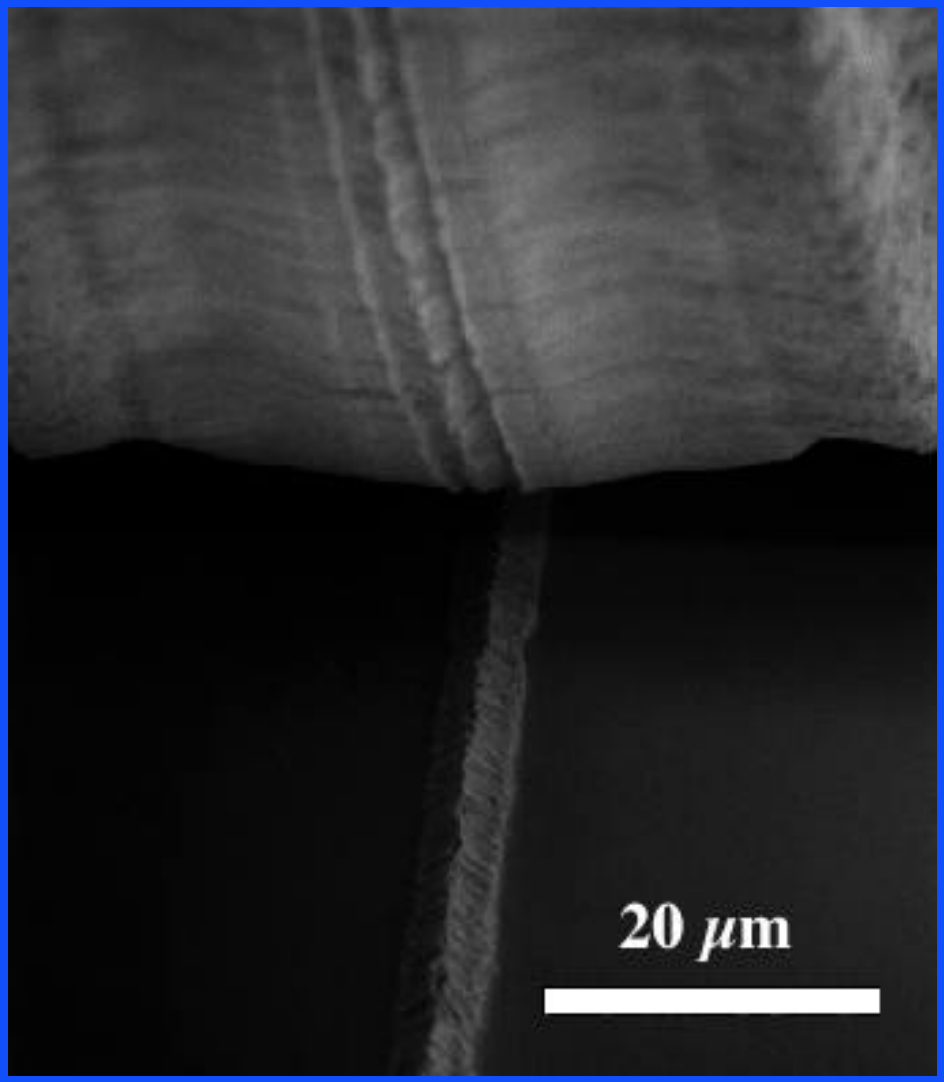


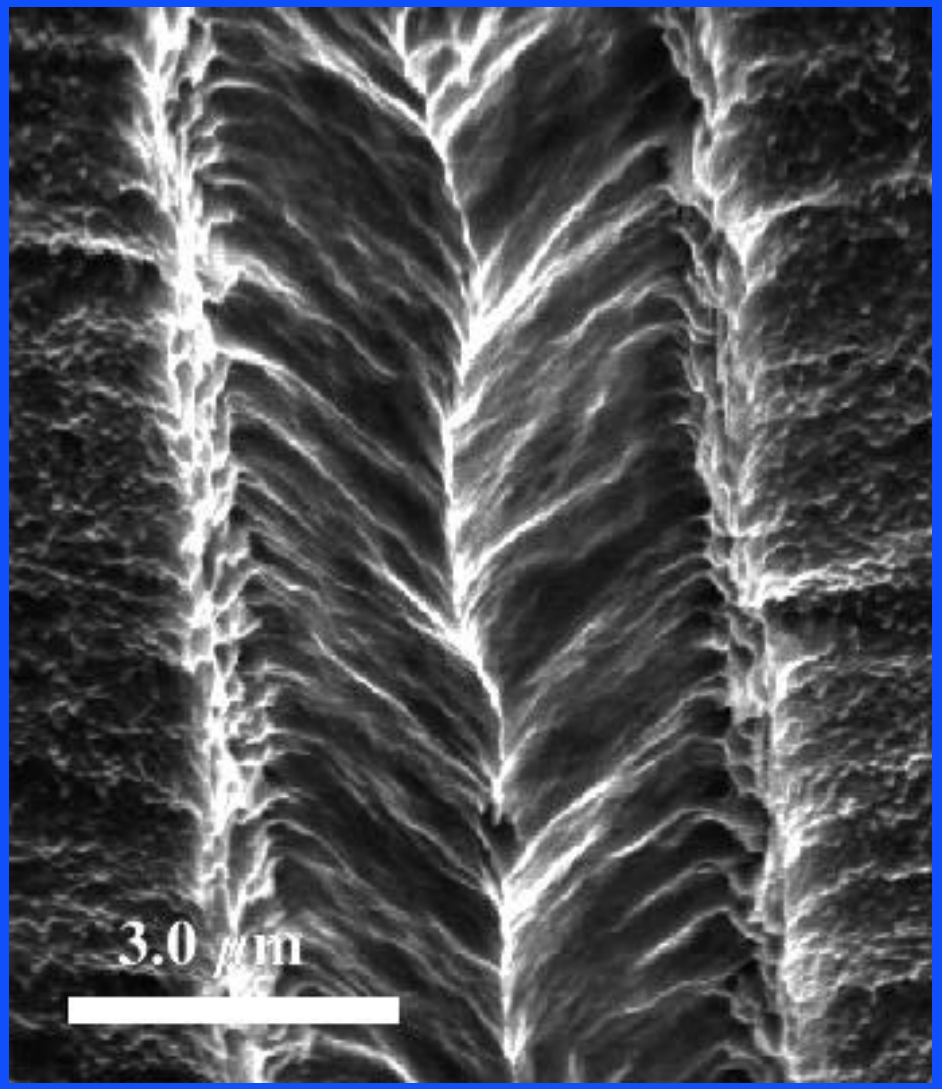
TEAR-OFF PLATED STRUCTURES



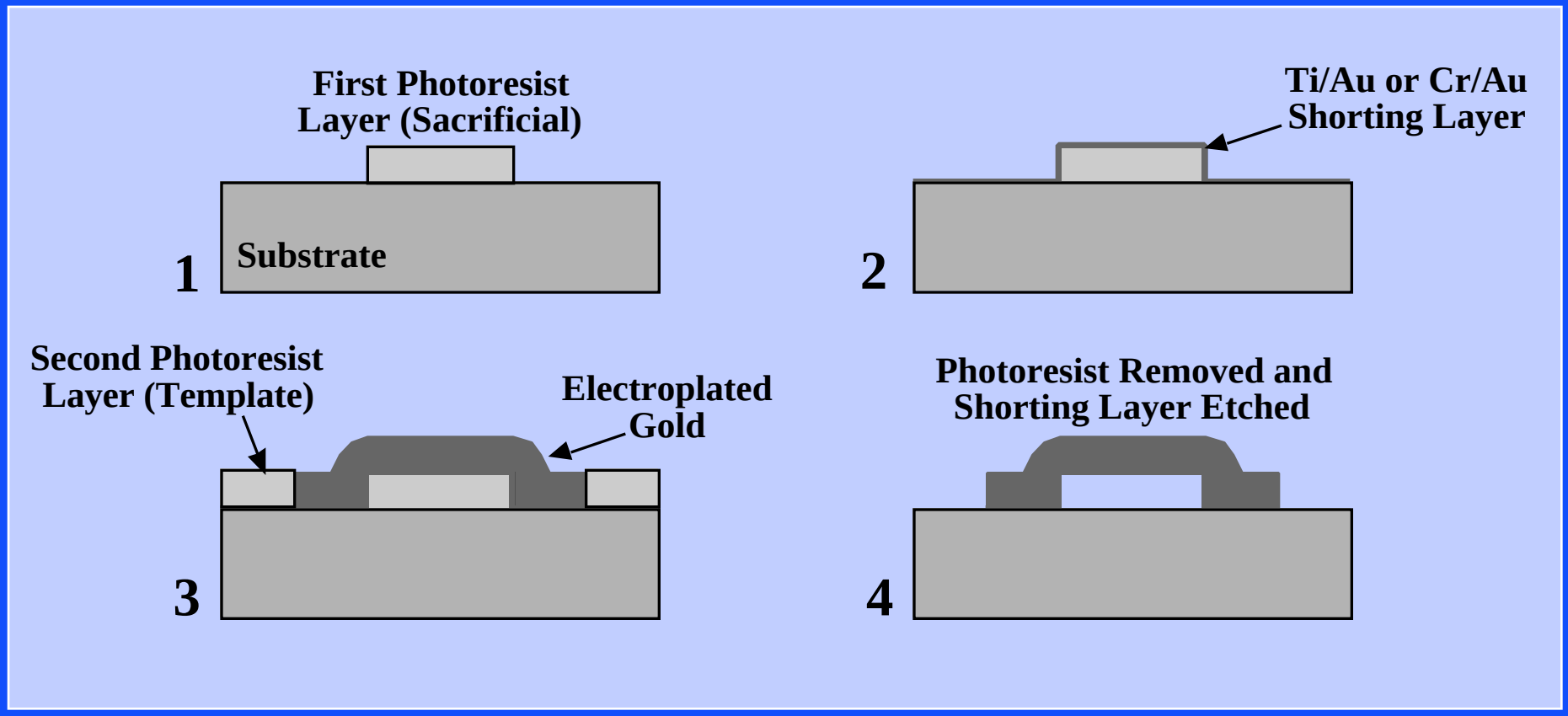


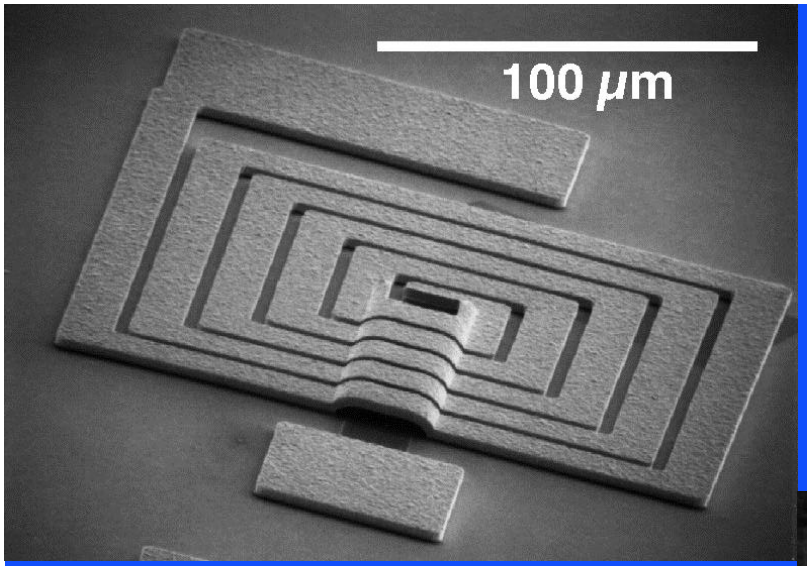






SACRIFICIAL LAYERS IN ELECTROPLATING

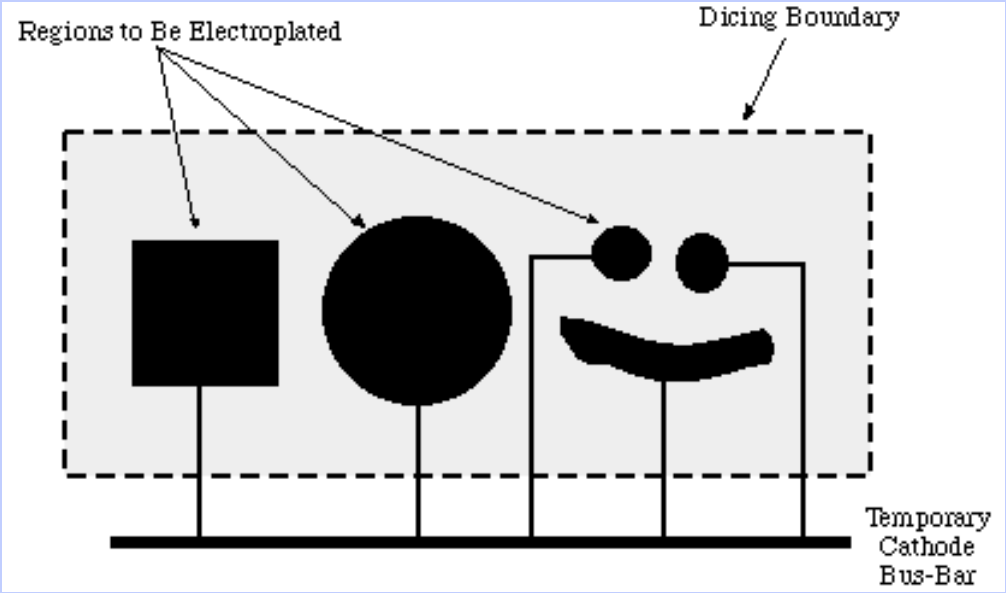




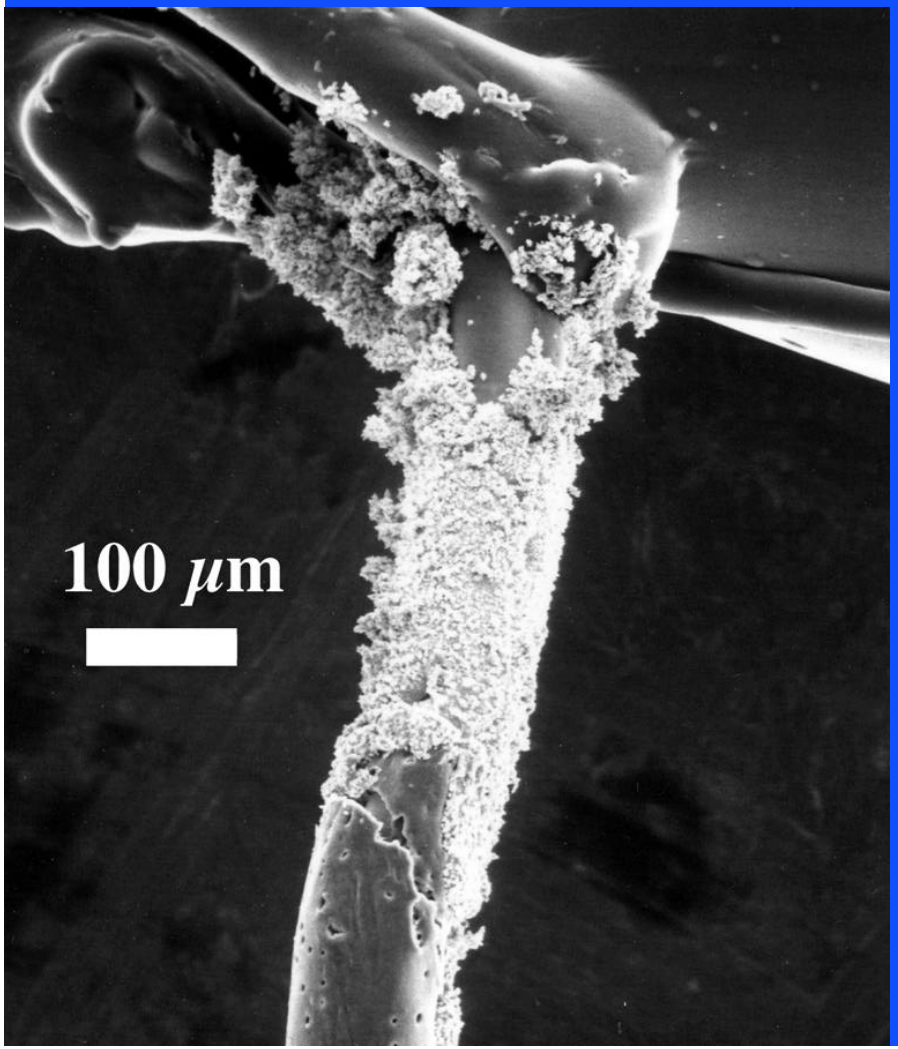
Electroplated Spiral Inductor with Air Bridges

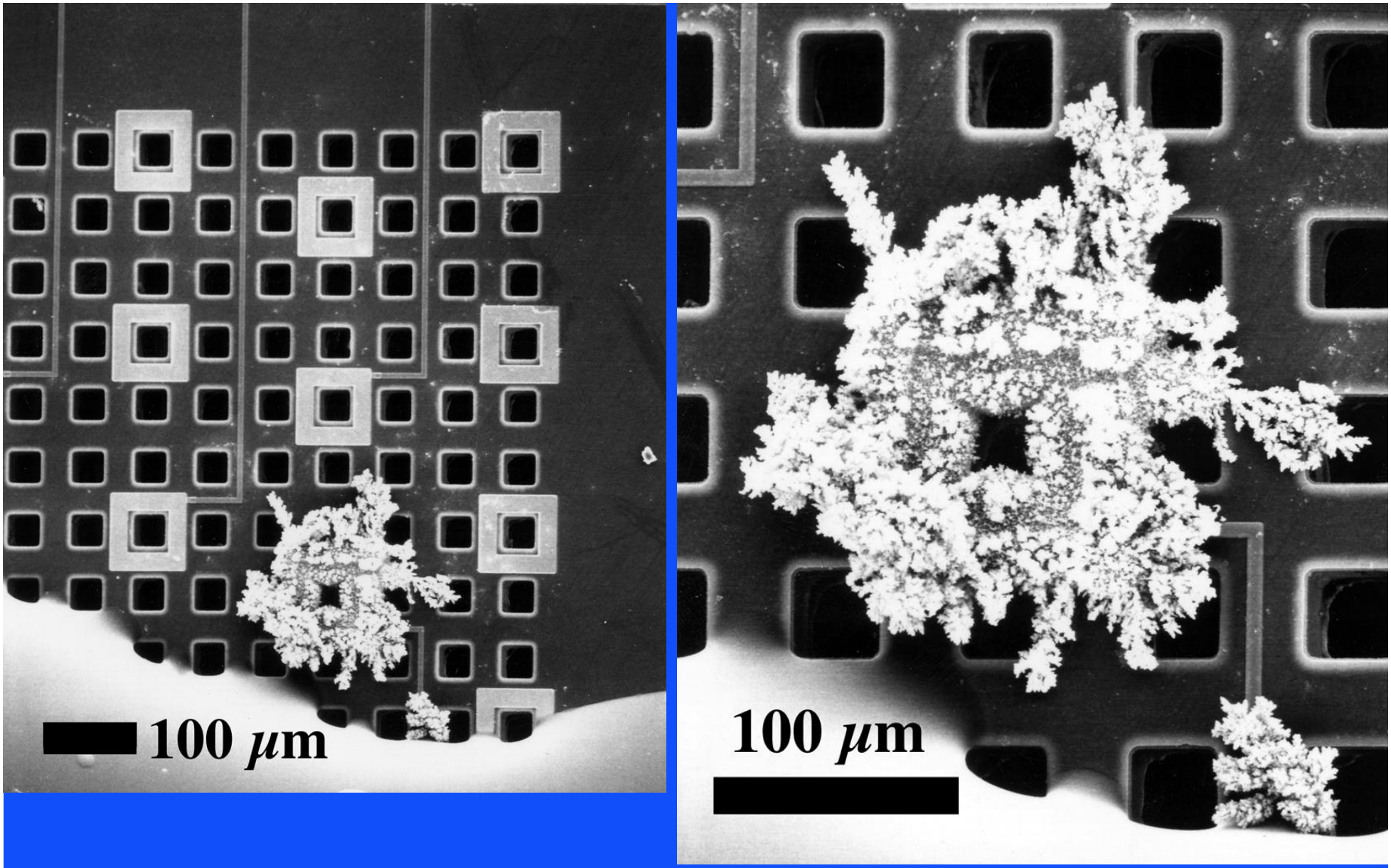
Images courtesy of C. W. Storment.

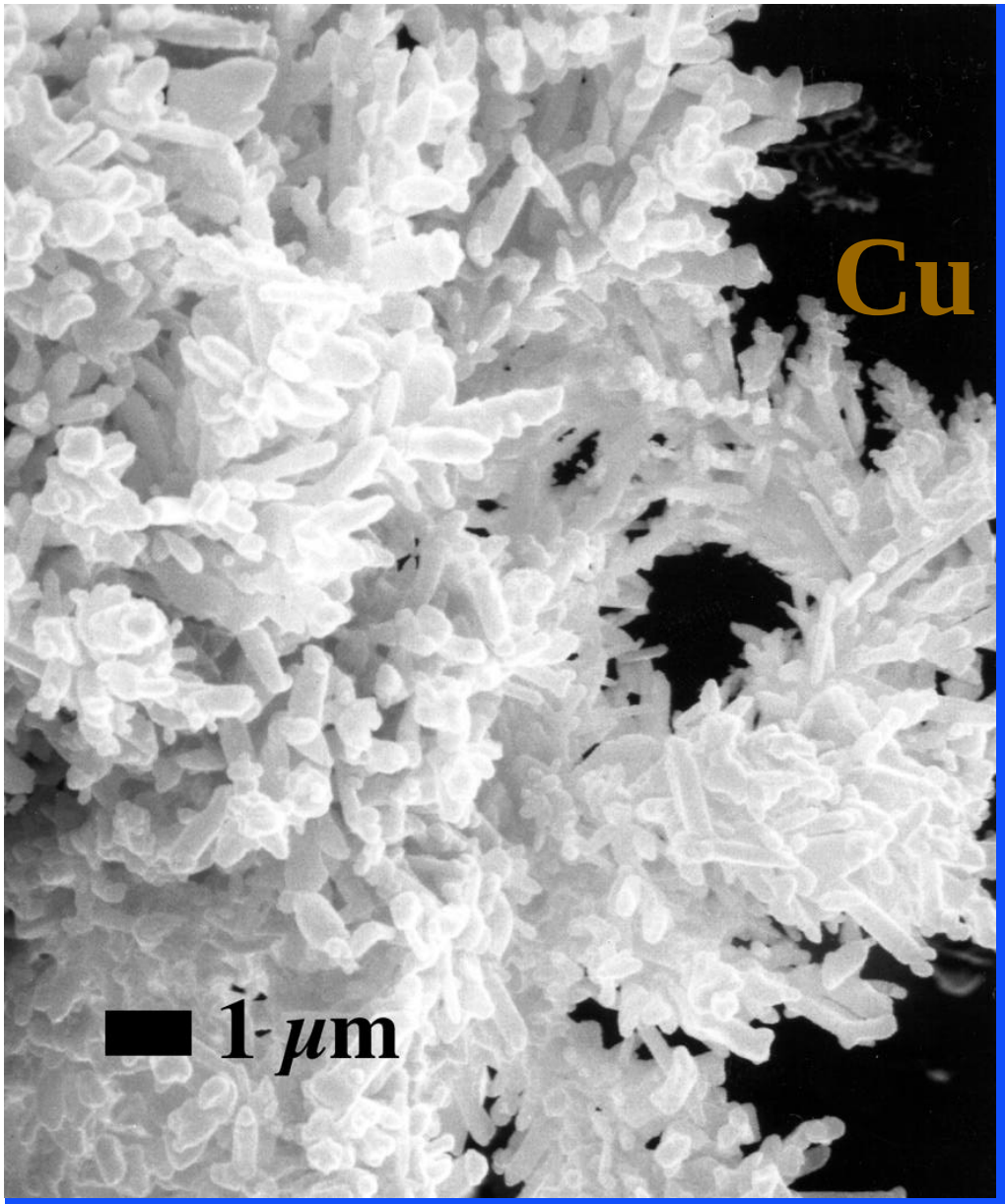
TEMPORARY SHORTING TRACES



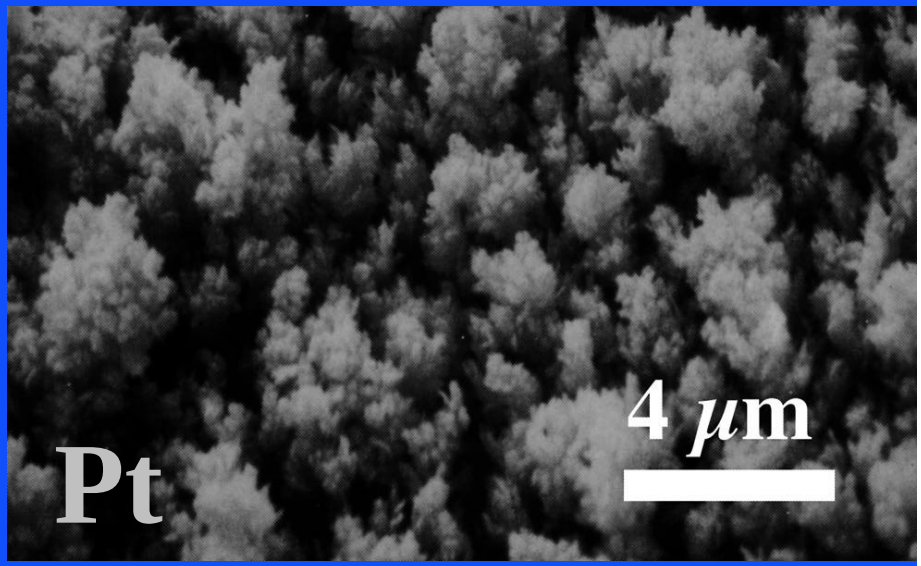
Electroplating to Map Defects





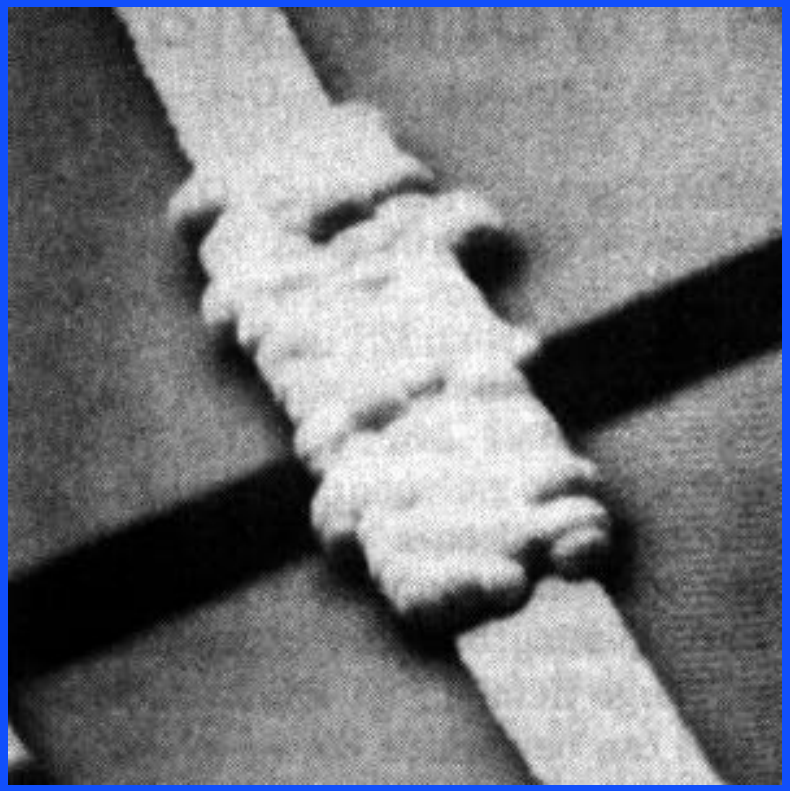


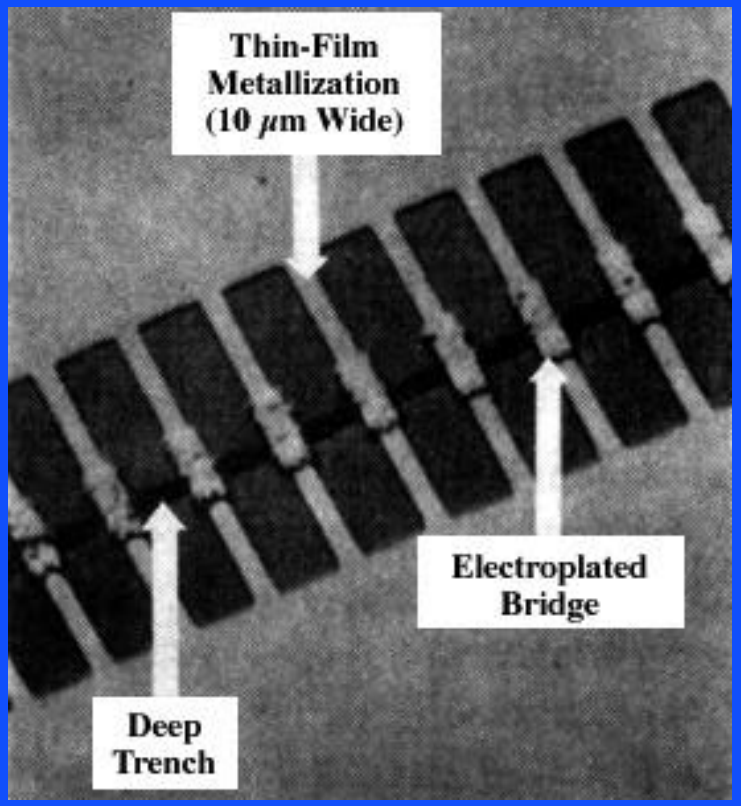
Ultra-Textured ("Black") Plated Metal



Source (above): Lang, W., Kühl, K., and Sandmaier, H., "Absorbing Layers for Thermal Infrared Detectors," Sensors and Actuators, vol. A34, no. 2, Sept. 1992, pp. 243 - 248.

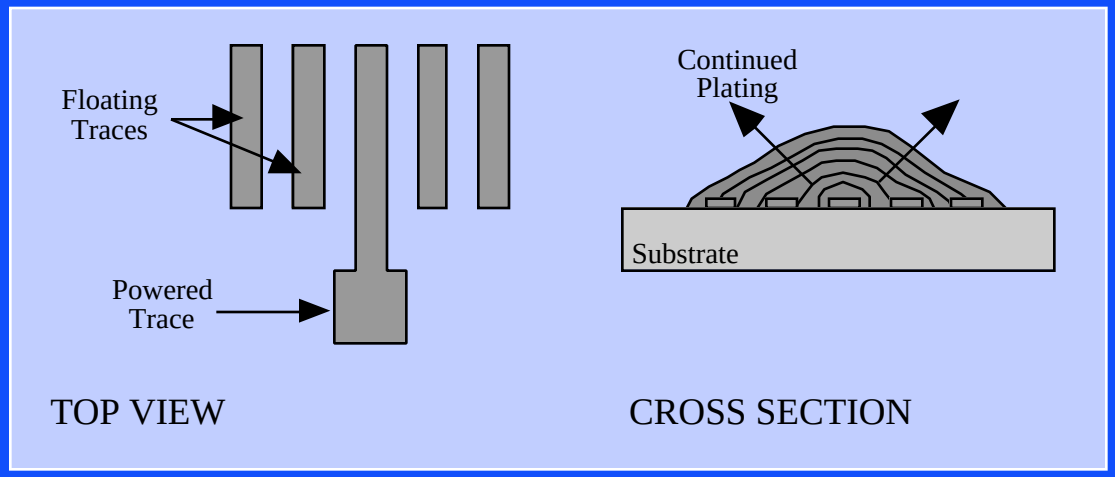
ELECTROPLATED INTERCONNECT CONCEPT



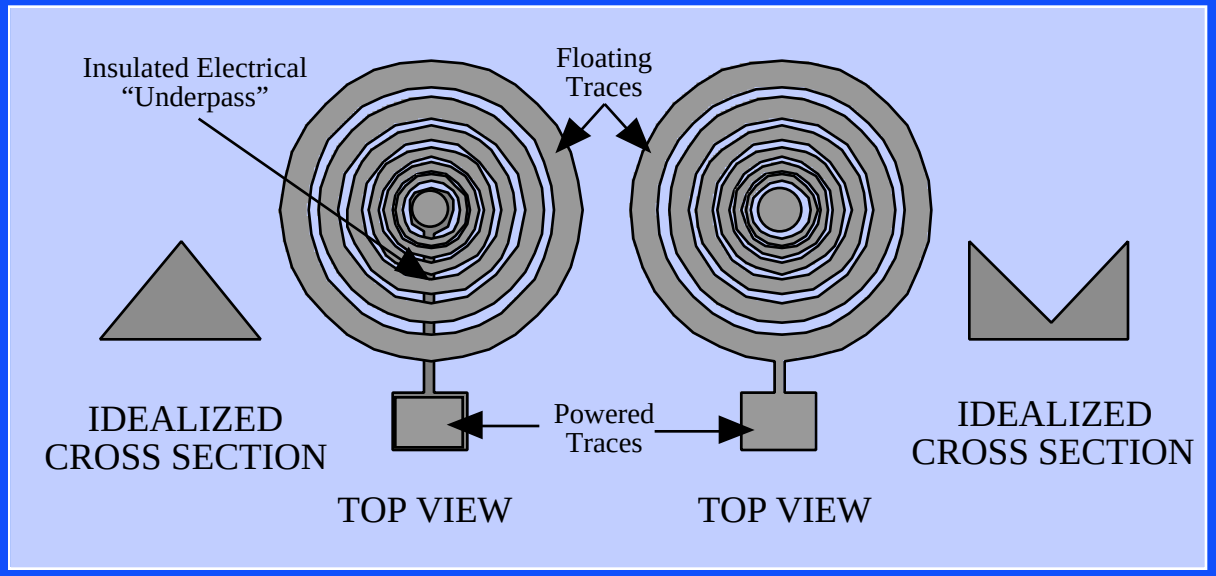


Source: Wu, S.-Y., "A Hybrid Mass-Interconnection Method by Electroplating," IEEE Transactions on Electron Devices, vol. ED-25, no. 10, Oct. 1978, pp. 1201 - 1203.

SELF-SHORTING TRACES



Top Figure After: Wagner, B., Reimer, K., Maciossek, A., and Hofmann, U., "Infrared Micromirror Array with Large Pixel Size and Large Deflection Angle," Proceedings of Transducers '97, the 1997 International Conference on Solid-State Sensors and Actuators, Chicago, IL, June 16 - 19, 1997, vol. 1, pp. 75 - 78.

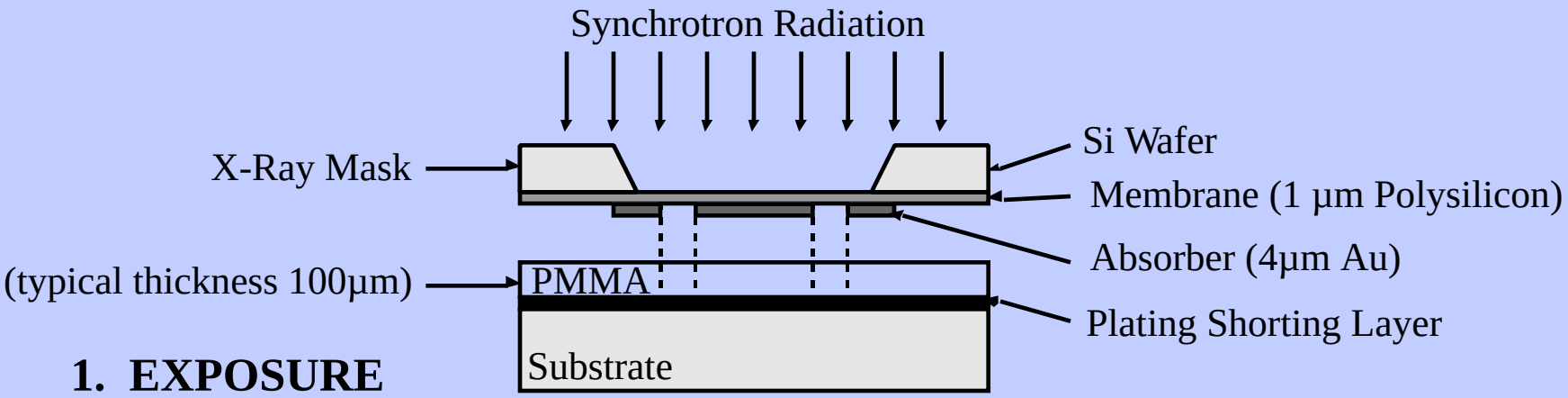


LITHOGRAPHIE, GALVANOFORMUNG, ABFORMUNG (LIGA)

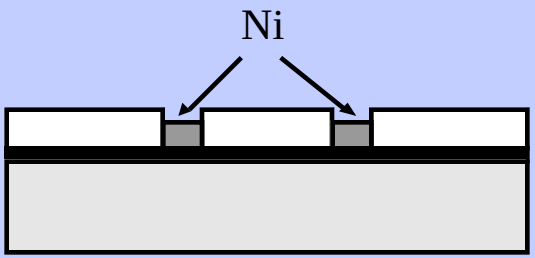
- The LIGA techniques uses synchrotron radiation (collimated x-rays) to expose polymethylmethacrlyate (PMMA) template layers.
- Metal can be plated into the template and 100:1 or better aspect ratios can be achieved.
- It is not easy to do and requires a synchrotron, but can produce some amazing structures.

Reference: Rogner, A., Eicher, J., Munchmeyer, D., Peters, R.-P., and Mohr, J., "The LIGA Technique - What Are the Opportunities?," Journal of Micromechanics and Microengineering, vol. 2, no. 3, Sept. 1992, pp. 133 - 140.

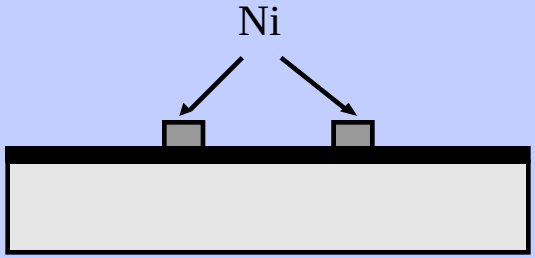
THE LIGA PROCESS



1. EXPOSURE

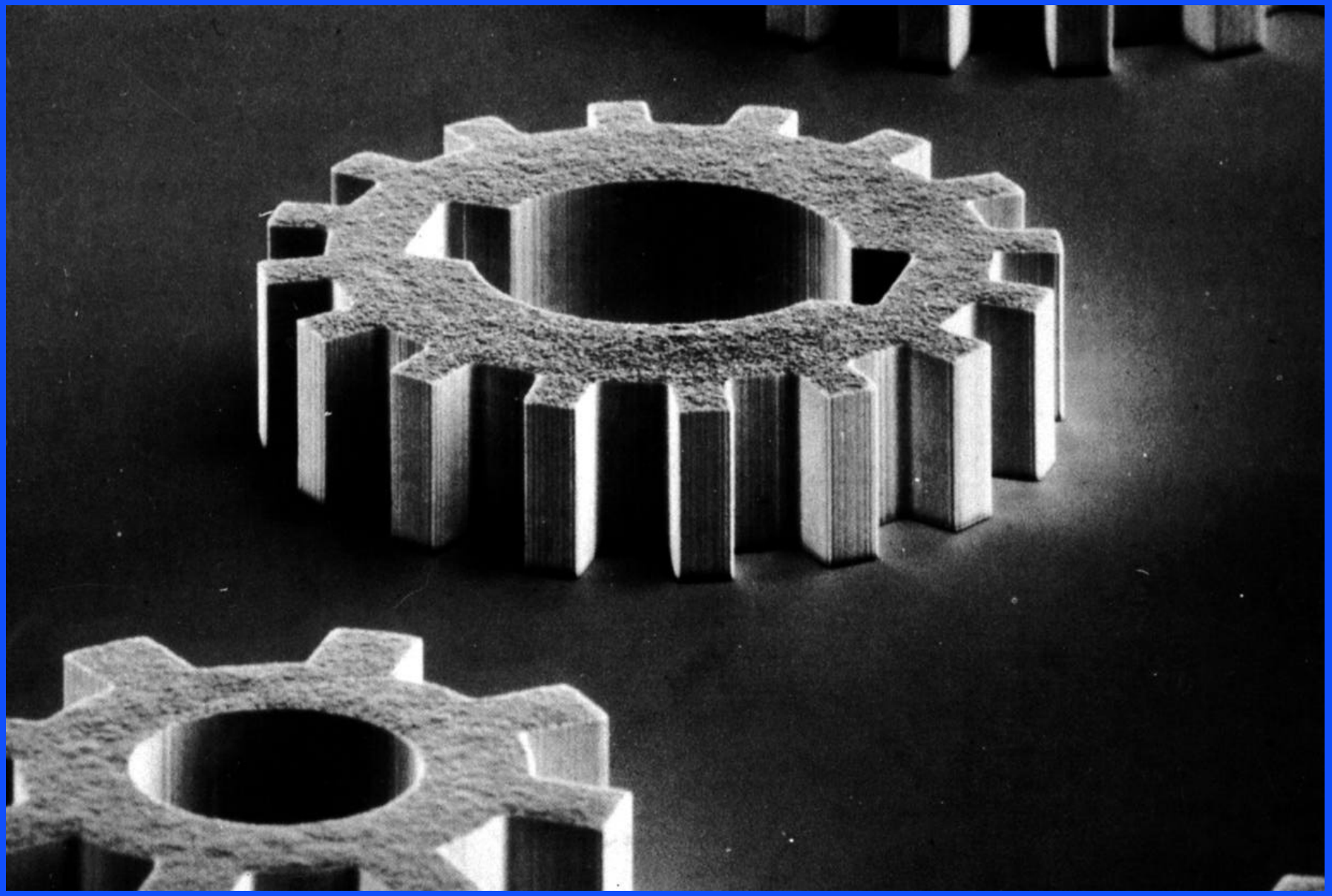


2. ELECTROPLATING



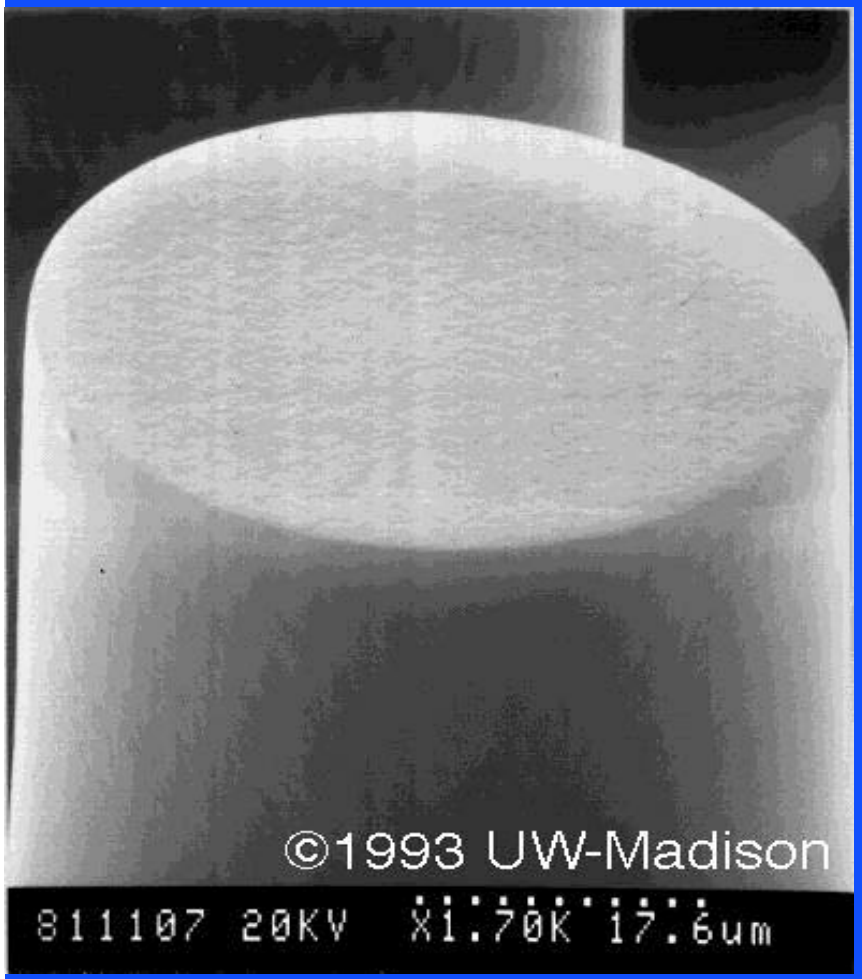
3. PMMA REMOVAL

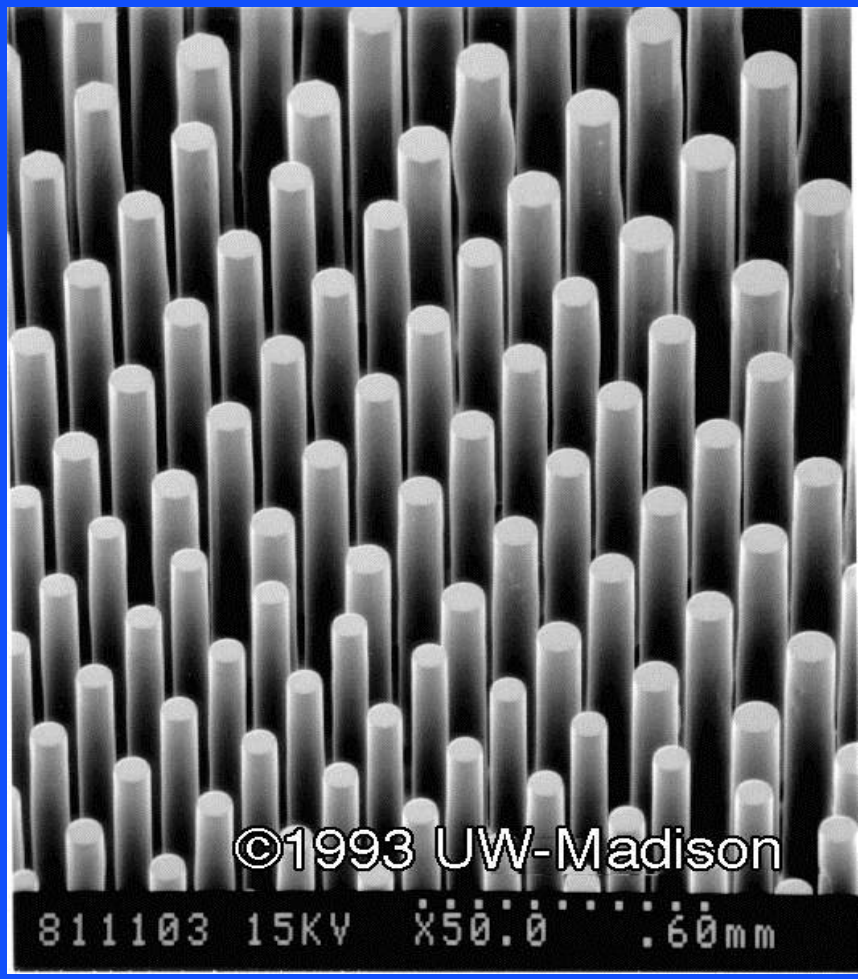
Courtesy of Prof. Henry Guckel



Courtesy of Prof. Henry Guckel

2 mm Tall LIGA Posts





Courtesy of Prof. Henry Guckel

http://mems.engr.wisc.edu/images/

SACRIFICIAL LAYER LIGA: SLIGA

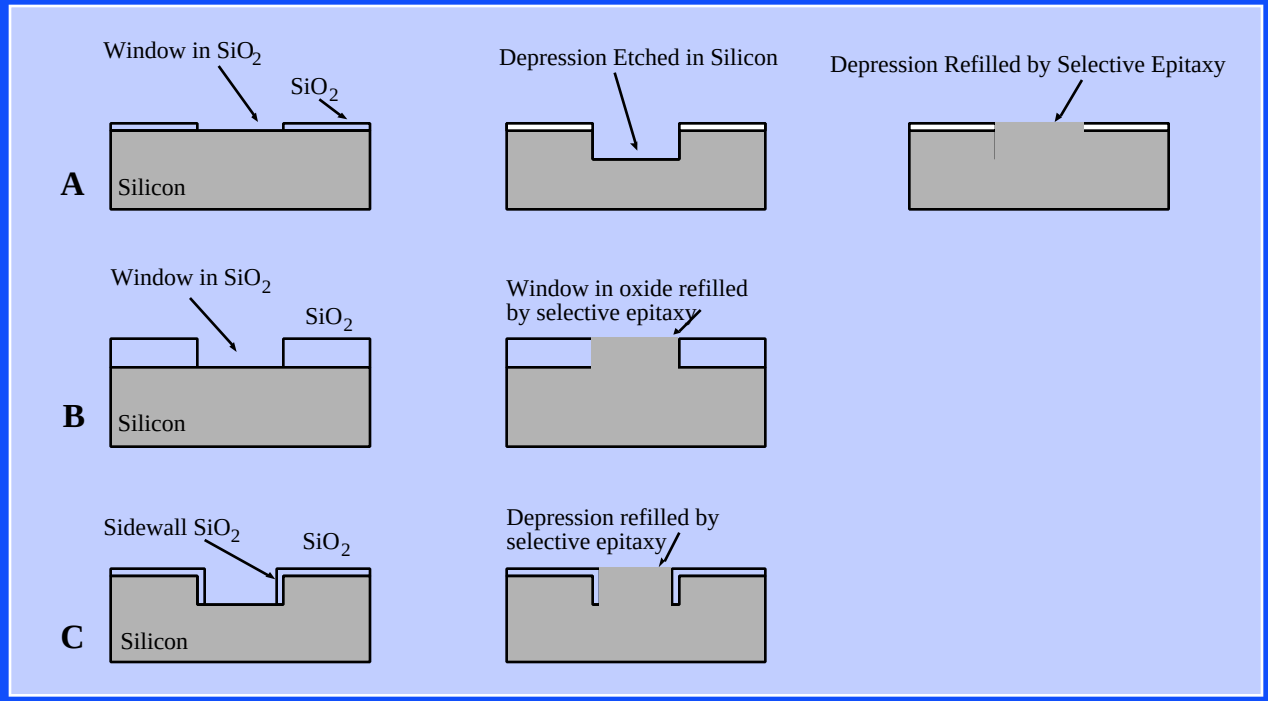
• **By combining a sacrificial layer with LIGA, moveable structures can be realized, such as the electrostatic comb drive shown.**

Courtesy of Prof. Henry Guckel

http://mems.engr.wisc.edu/images/

SELECTIVE EPITAXIAL GROWTH

- **Epitaxial silicon can be grown selectively (single crystal on exposed silicon and polycrystalline silicon on oxide) to form mesas and filled pits selectively.**
- **Adding HCl to the reactants removes polysilicon as it forms, leaving epitaxial silicon.**

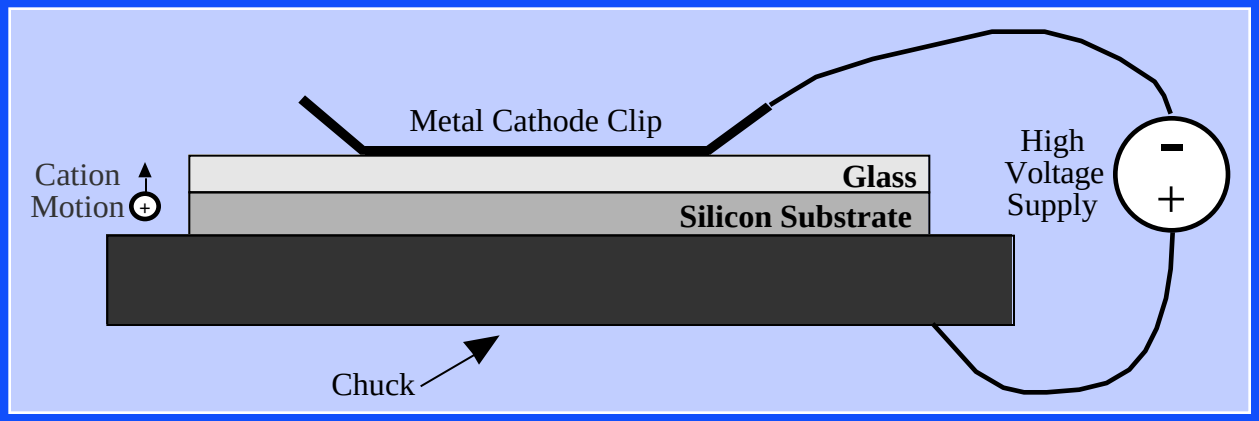


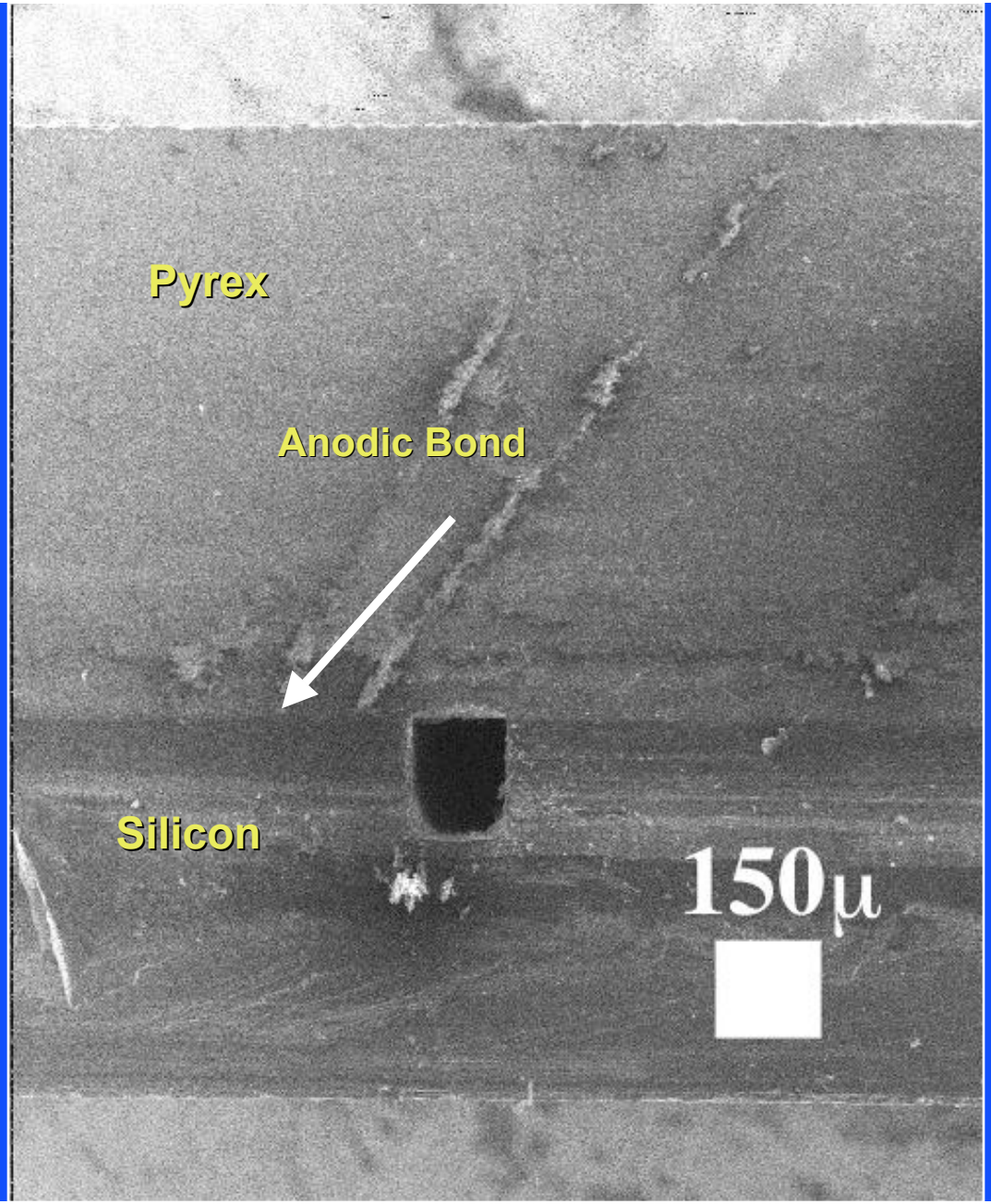
BONDING PROCESSES

- **Anodic bonding can be used to bond silicon to glass or other materials with glass layers.**
- **Fusion bonding is a high-temperature process for bonding silicon wafers together (often used to form vacuum cavities, membranes, cantilevers, etc.). Pits are often pre-etched into one wafer.**
- **Adhesive bonding can also be useful in micromachining.**

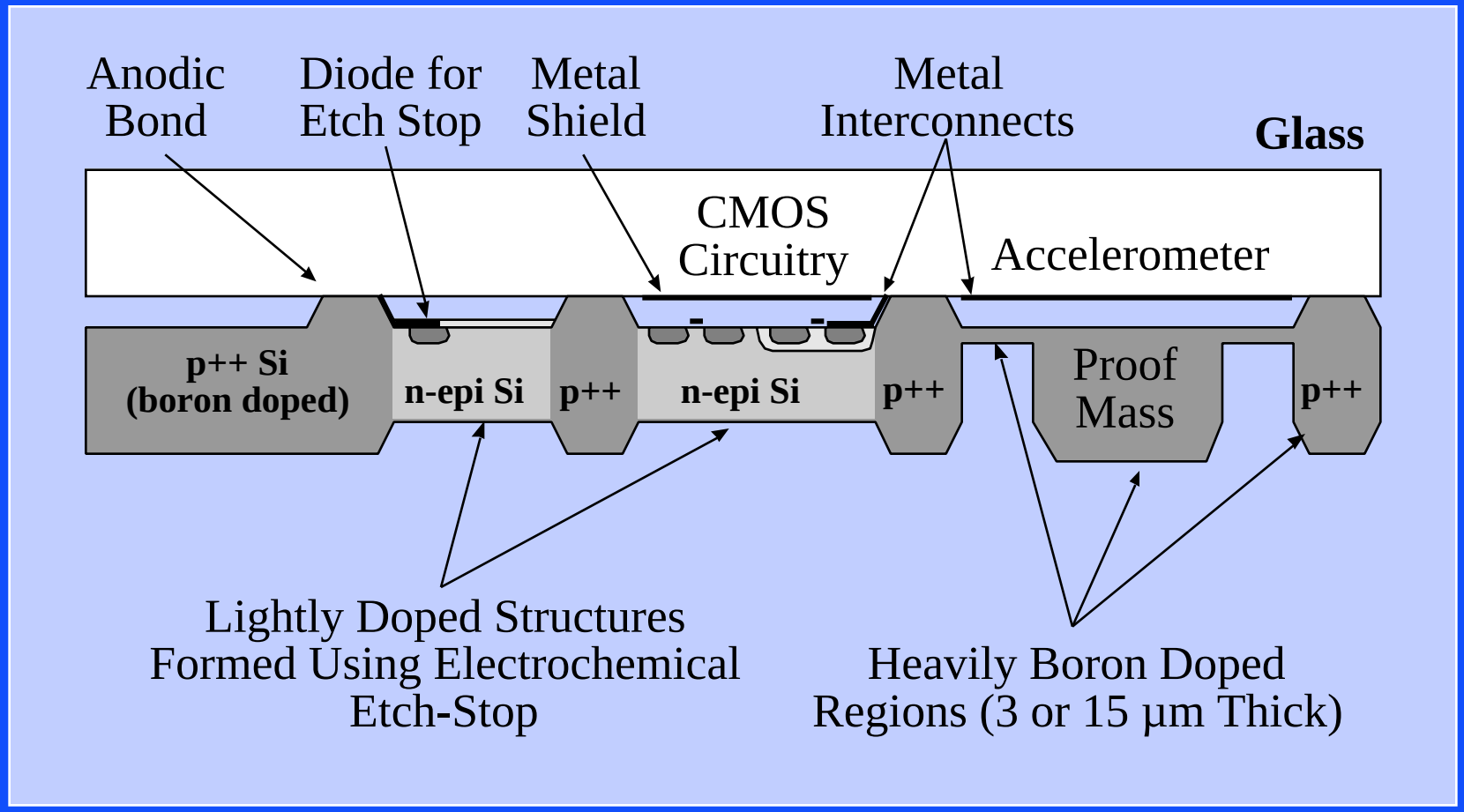
ANODIC BONDING

- Under applied potential, positive ions in the glass move toward negative potential (anode) and produce a large field at the glass-silicon interface.
- The field pulls the surfaces together, facilitating covalent bond formation.
- The bonds are hermetic and very strong, and thin metal traces can be sealed between the surfaces and maintain hermeticity.
- Glass can be sputtered onto another wafer silicon to allow anodic bonding.





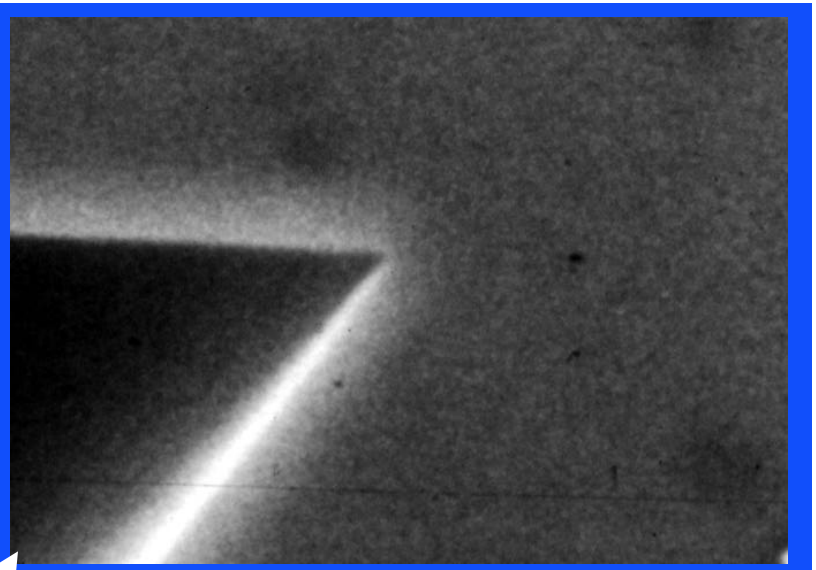
ANODIC BONDING BASED COMPOUND PROCESS

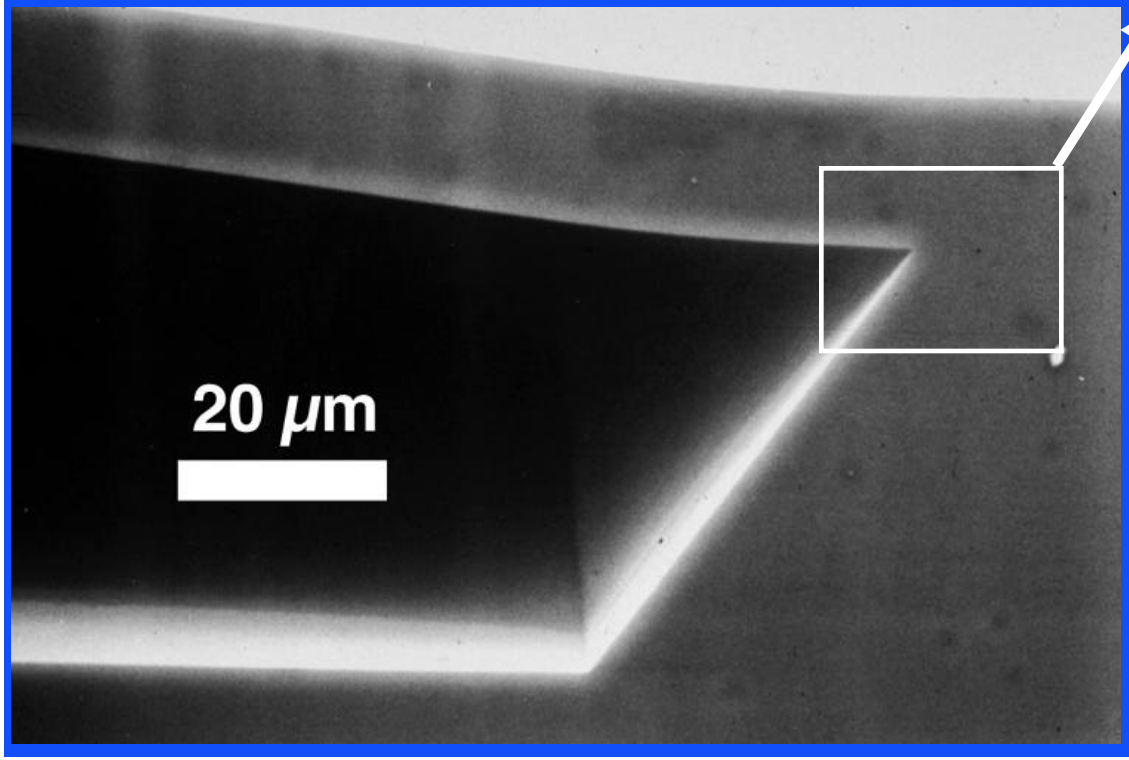


Reference: Gianchandani, Y. B., Ma, K. J., and Najafi, K., "A CMOS Dissolved Wafer Process for Integrated P++ Microelectromechanical Systems," Proceedings of Transducers '95/Eurosensors IX, Stockholm, Sweden, June 25 - 29, 1995, vol. 1, pp. 79 - 82.

FUSION BONDING

- **Direct silicon-to-silicon bonds, sharing oxygen atoms between wafers.**
- **Carried out at high temperature (300 - 800°C).**

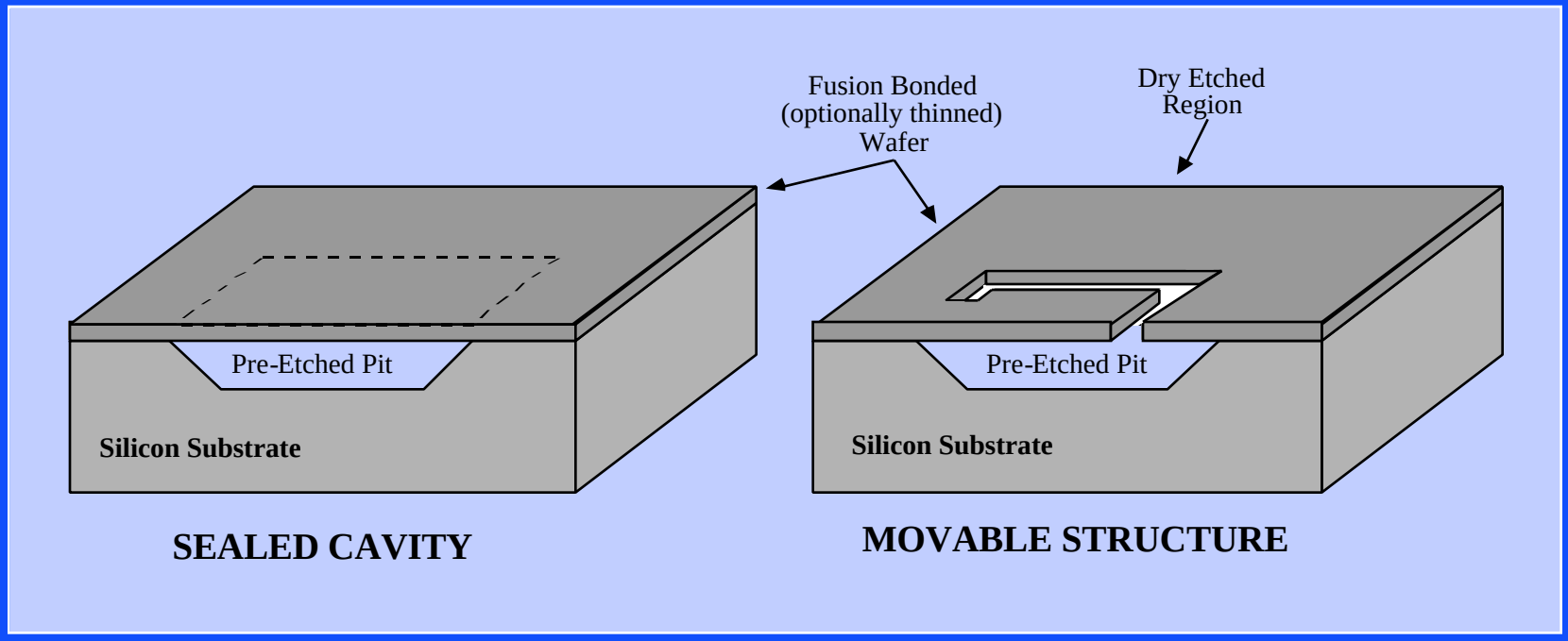




Postulated Reaction: Si-O-H + H-O-Si –> Si-O-Si + H_2O

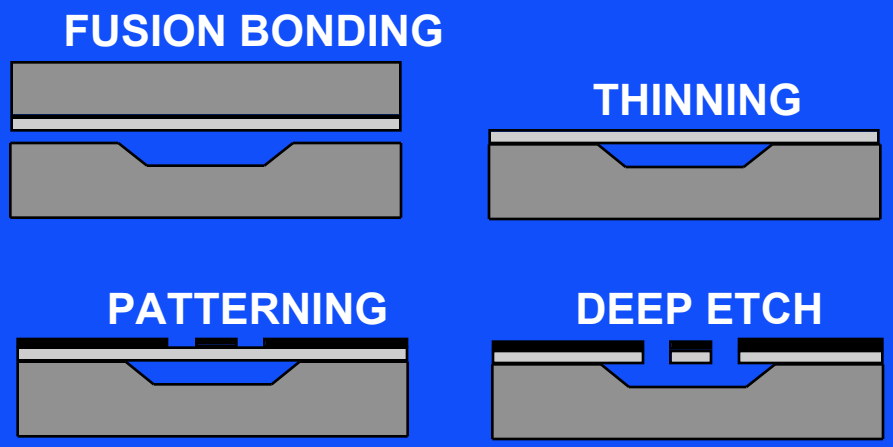
Courtesy of Prof. Kurt Petersen, Lucas NovaSensor.

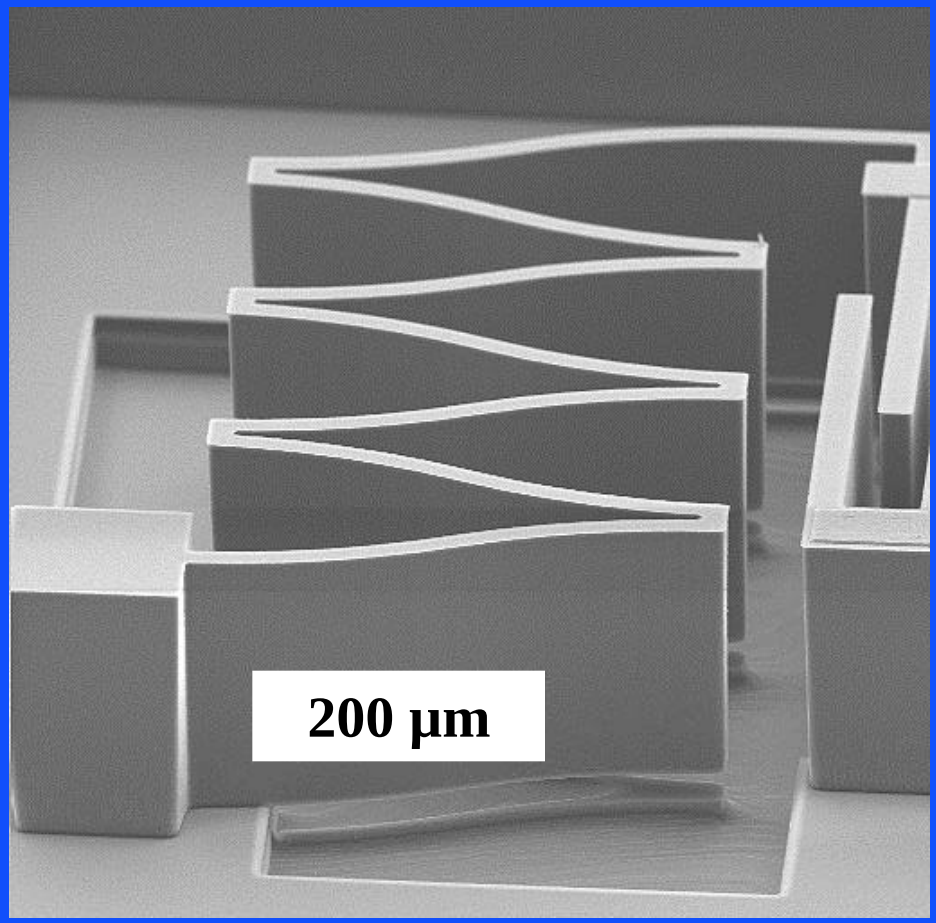
FUSION BONDING WITH PREFABRICATED PITS



DRIE + FUSION BONDING

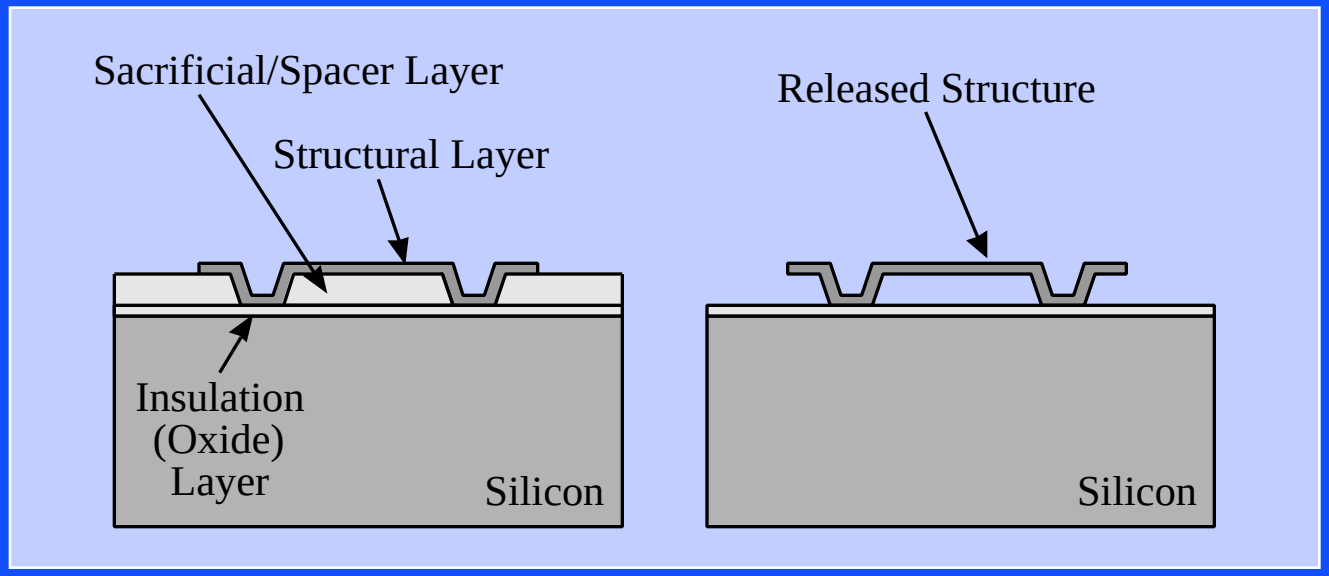
- **Combination of fusion bonding (with pre-etched cavities) and deep RIE (DRIE).**



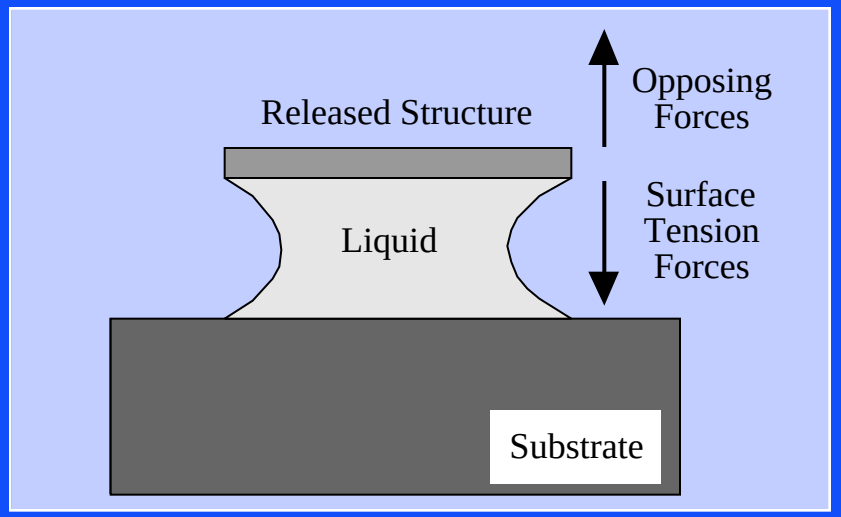


SACRIFICIAL PROCESSES

- **Temporary spacer layers (“sacrificial layers”) are used initially and later etched away to form moving structures and/or cavities (cavities can later be sealed).**
- **Sticking during wet release can be a big problem (surface treatments, sublimation and critical point drying are used for improving yield).**



WET RELEASE ISSUES



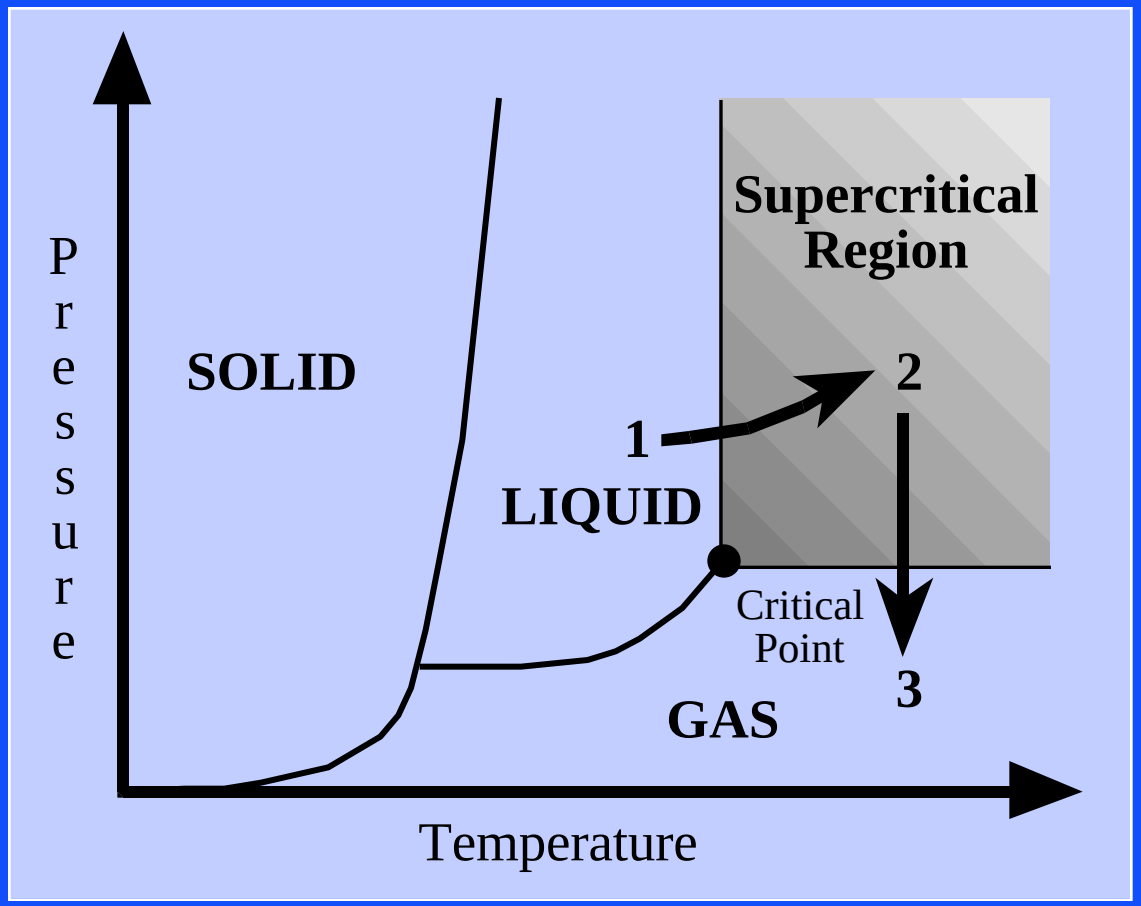
- van der Waals forces (attractive and repulsive electrostatic dipole-dipole interactions between molecules) are responsible for the stiction of hydrophobic surfaces.
- Hydrogen bonding (a particularly strong attraction between a hydrogen atom of one molecule and a pair of unshared electrons of another molecule) is the dominant adhesion mechanism for hydrophilic surfaces.
- Critical point and sublimation methods can help in some cases.
- Geometrical approaches and surface modification can also help.

FREEZE-DRY RELEASES

Source: Takeshima, N., Gabriel, K. J., Ozaki, M., Takahashi, J., Horiguchi, H., and Fujita, H., "Electrostatic Parallelogram Actuators," Proceedings of Transducers '91, the 1991 International Conference on Solid-State Sensors and Actuators, IEEE Press, San Francisco, CA, June 24 - 27, 1991, pp. 63 - 66.

- Simple hardware is required for this approach.
- The aqueous etchants are displaced by a high freezing-point alcohol such as t-butyl alcohol.
- Once frozen, the alcohol can be sublimed (direct transition to gas phase) with a simple vacuum system.

CRITICAL POINT DRYING

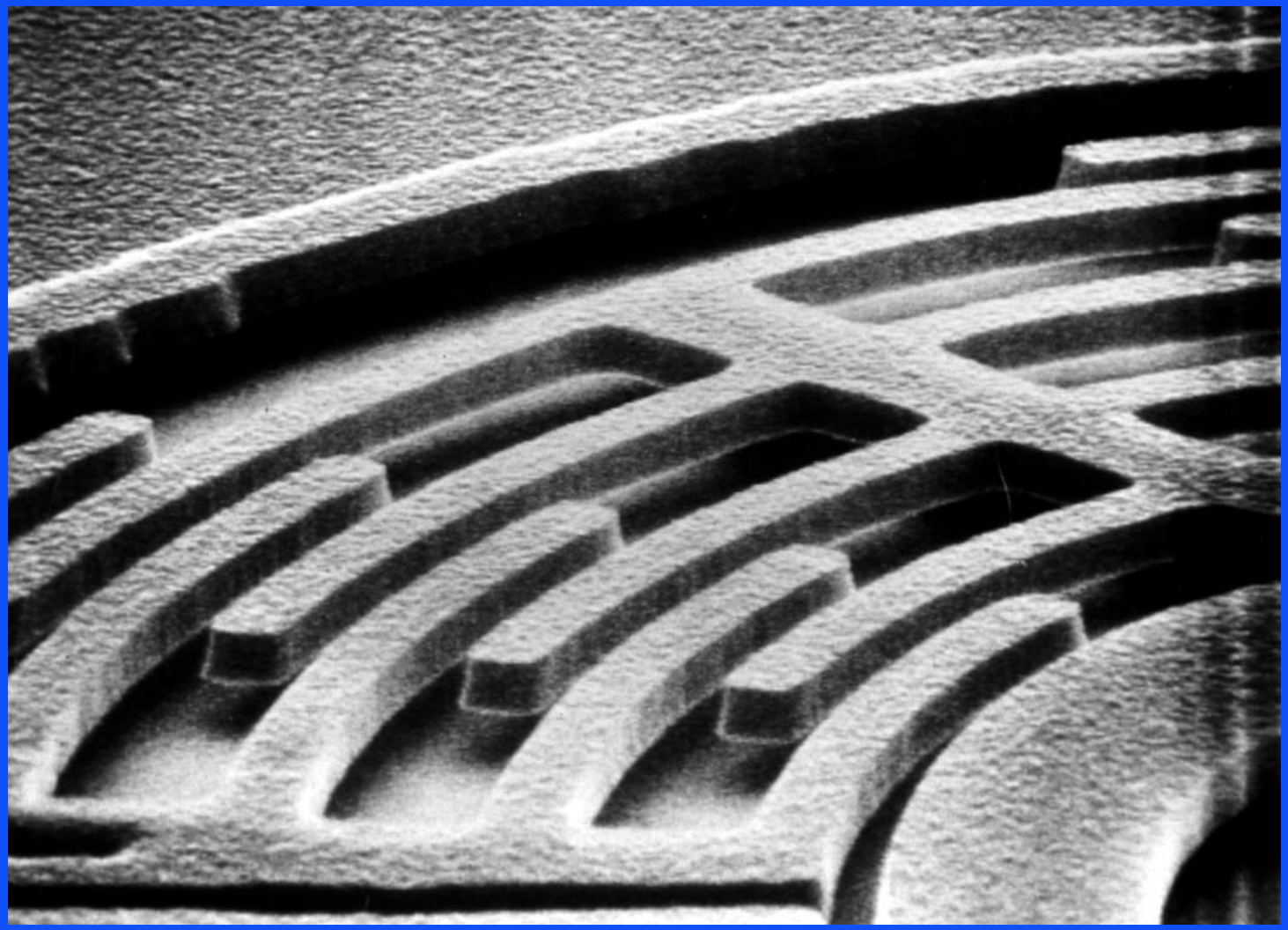


After Mulhern, et al., (1993).

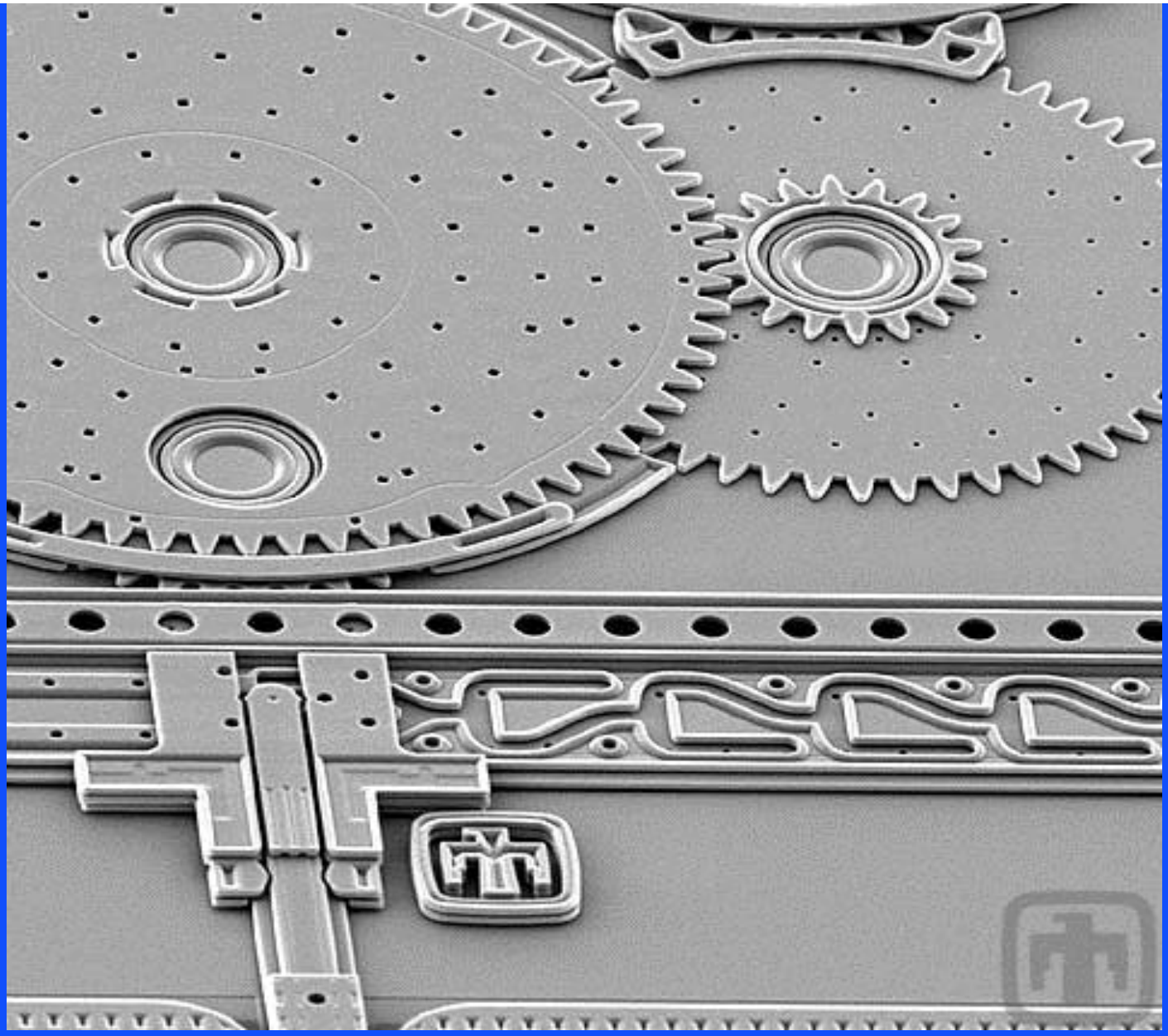
SURFACE MICROMACHINED STRUCTURES

- Generally this refers to thin-film structures fabricated above a substrate, generally using sacrificial layers that are etched, forming cavities or releasing moving regions of the films.
- Polysilicon microstructures (moving members, hinges, gears, etc.) can be used to fabricate a broad range of devices, generally using silicon dioxide or phosphosilicate glass sacrificial layers.
- Aluminum microstructures can be used to fabricate a complementary set of devices and do not require the high temperatures nor wet etching of polysilicon processes (organic sacrificial layers such as photoresist or polyimide are generally used).

POLYSILICON SURFACE MICROMACHINED DEVICES

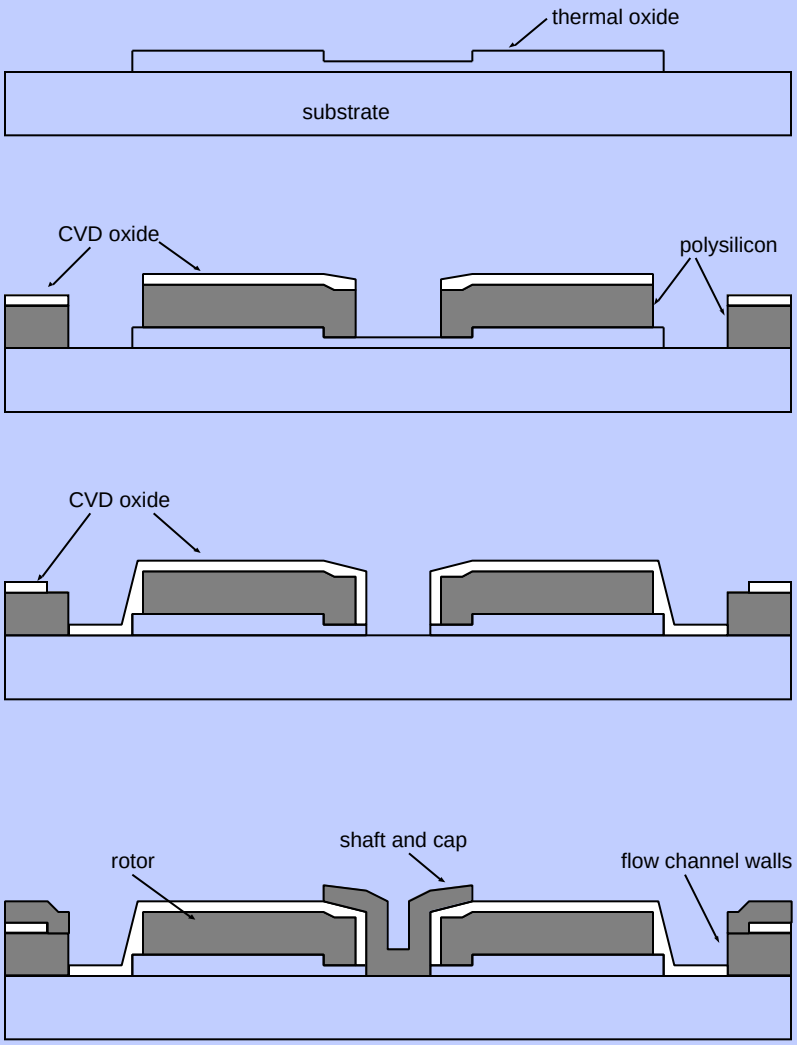


Courtesy Prof. R. Howe, U.C. Berkeley.

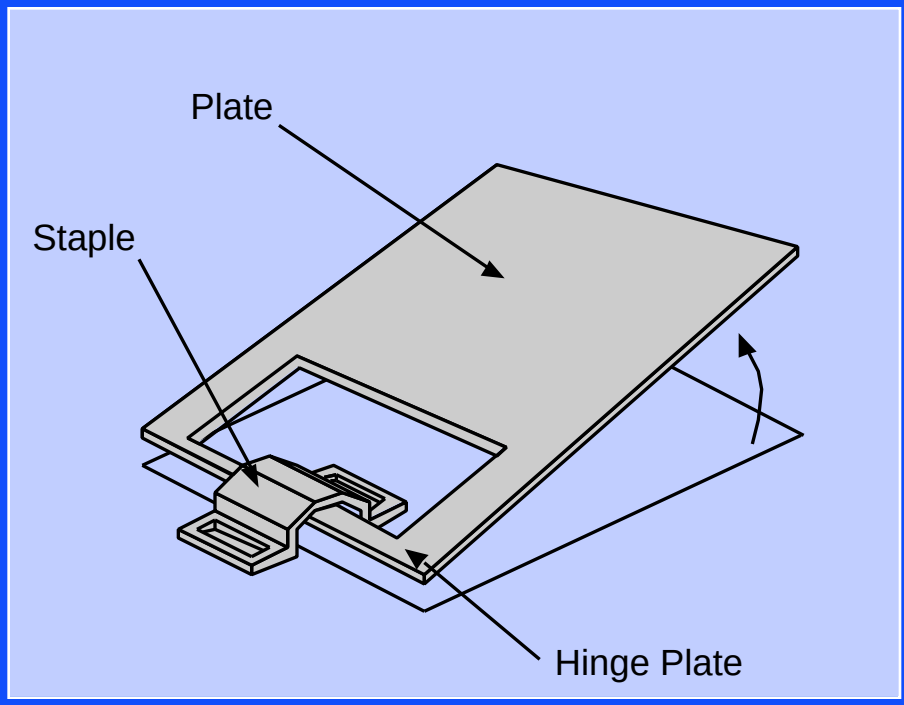


http://www.mdl.sandia.gov/Micromachine/images.html

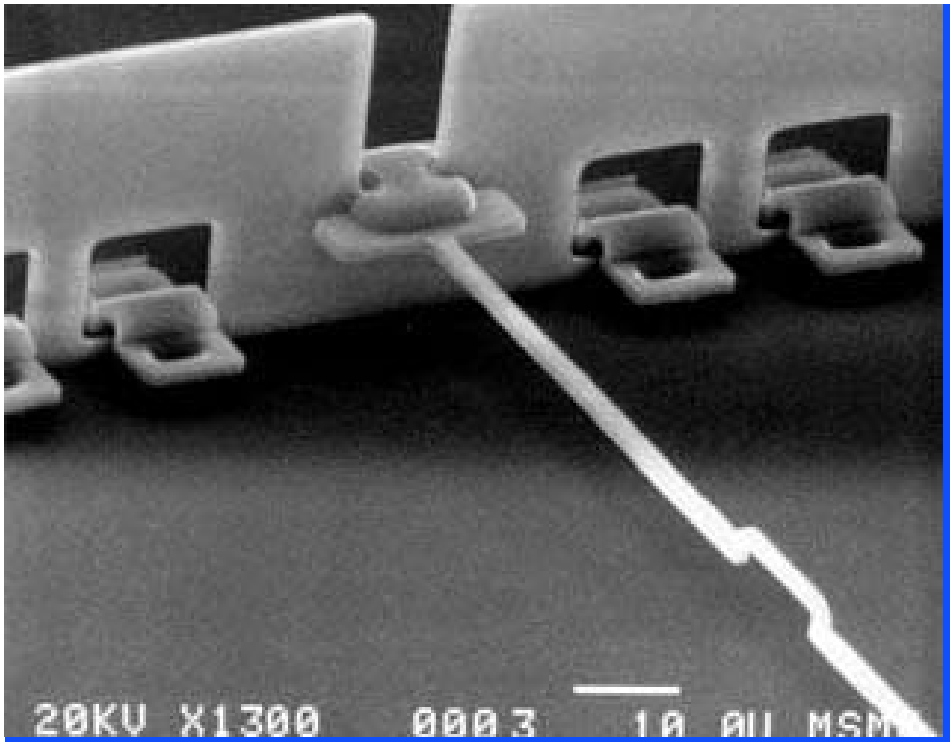
POLYSILICON STRUCTURES

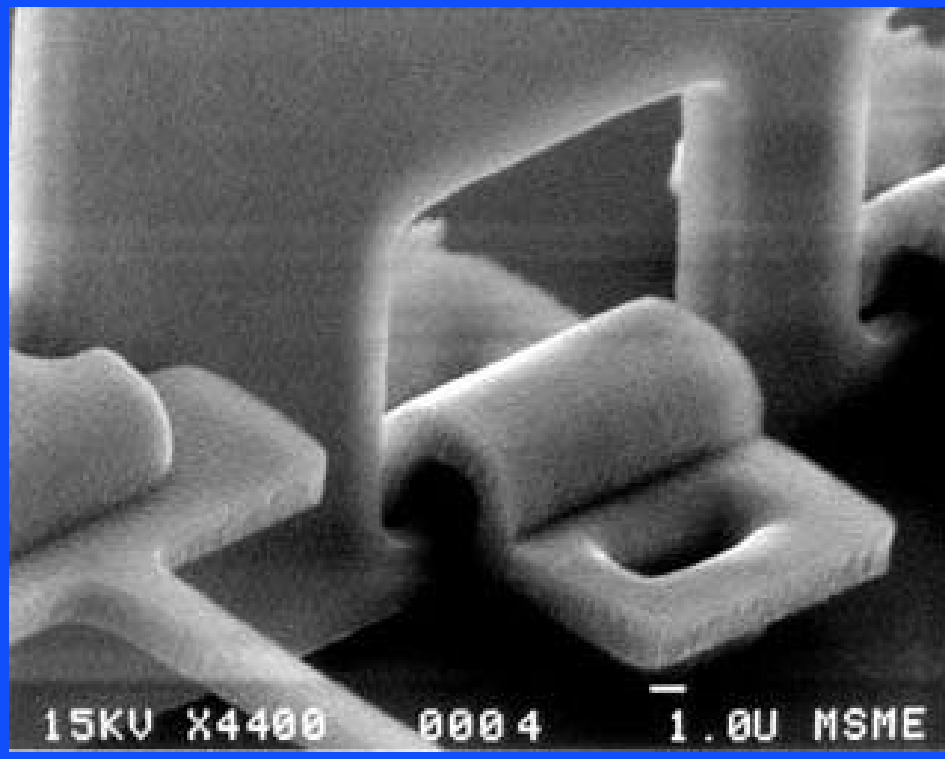


Reference: Mehregany, M., Gabriel, K. J., and Trimmer, W. S. N., "Integrated Fabrication of Polysilicon Mechanisms," IEEE Transactions on Electron Devices, vol. 35, no. 6, June 1988, pp. 719 - 723.

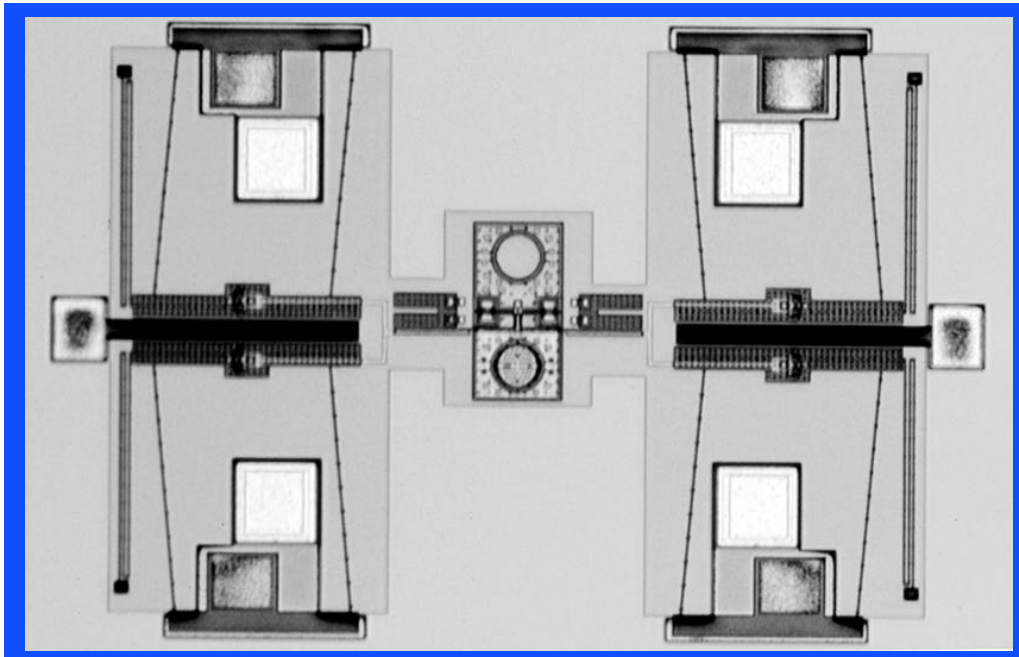


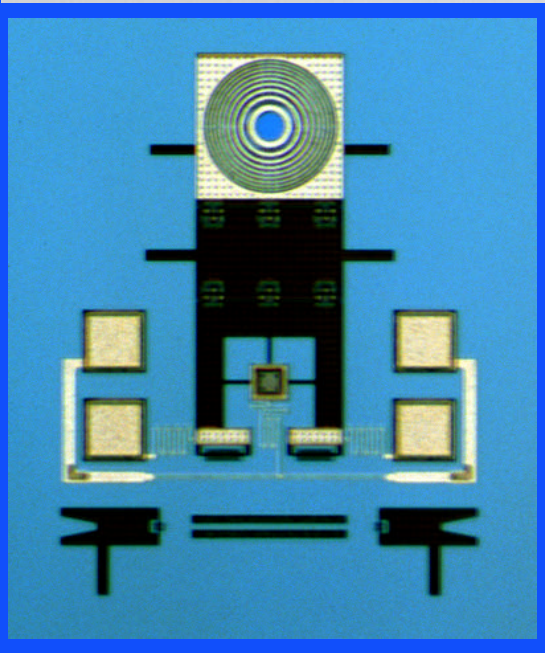
Reference: Pister, K. S. J., et al., "Microfabricated Hinges," Sensors and Actuators A, vol. A33, no. 3, June 1992, pp. 249 - 256.

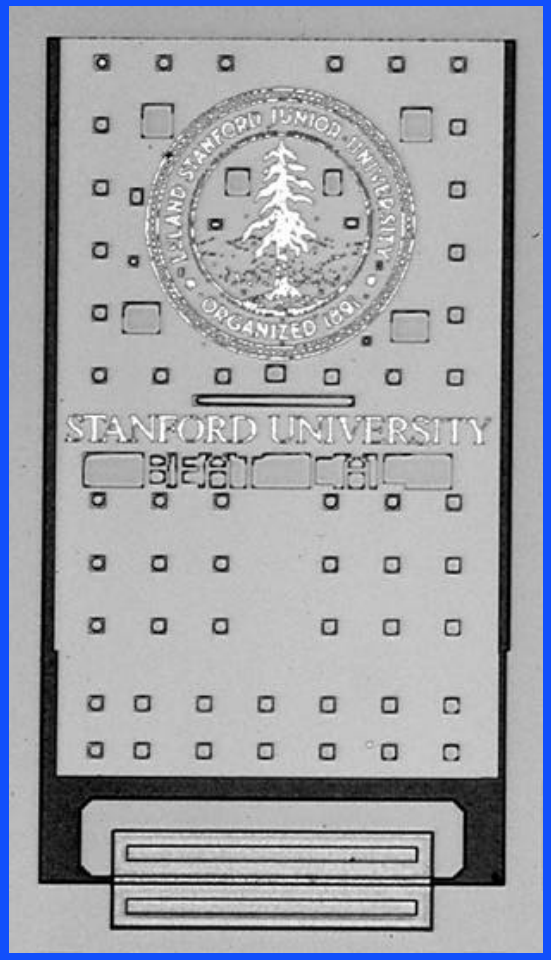




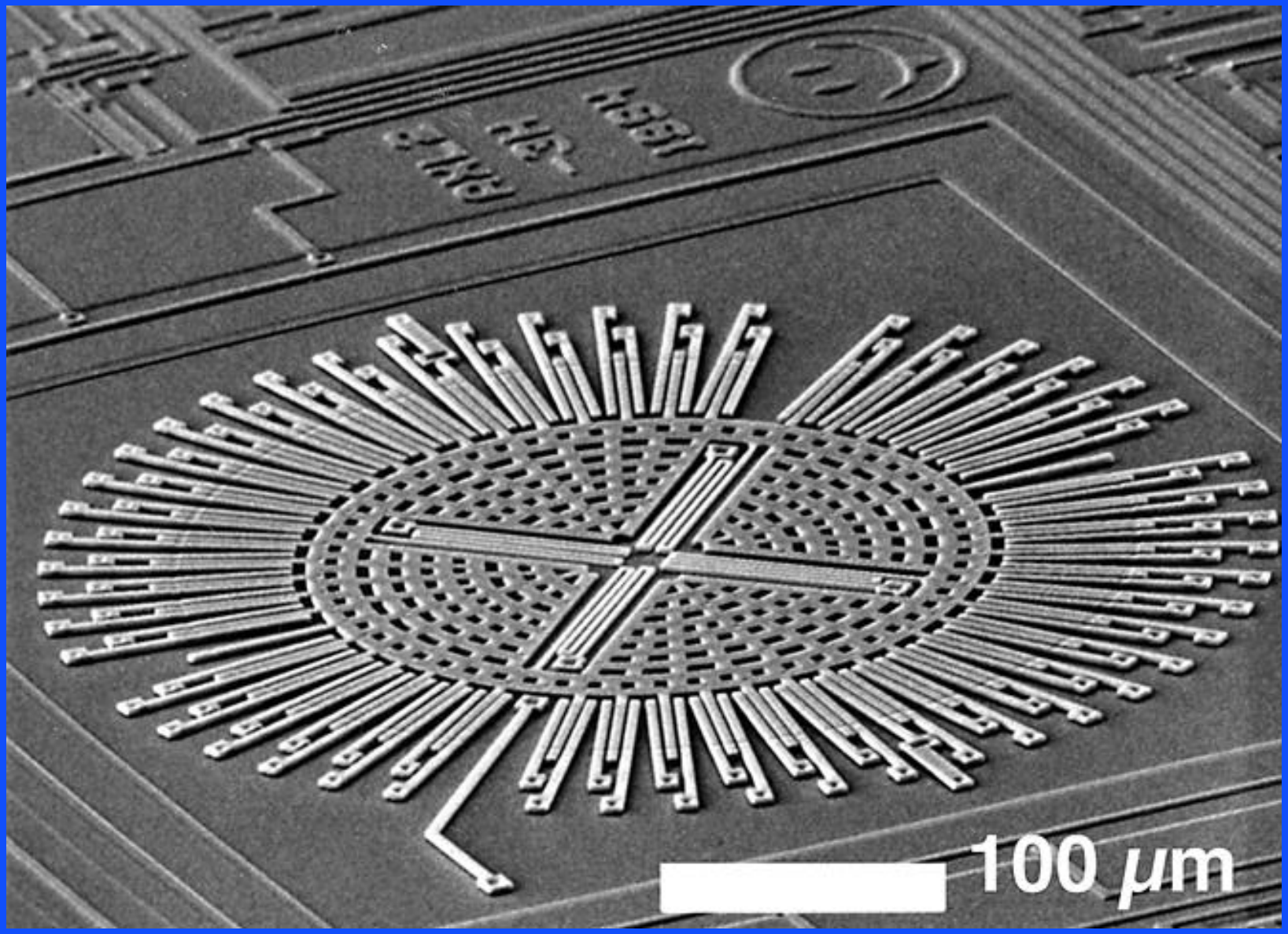
Courtesy M. Last, U. C. Berkeley.







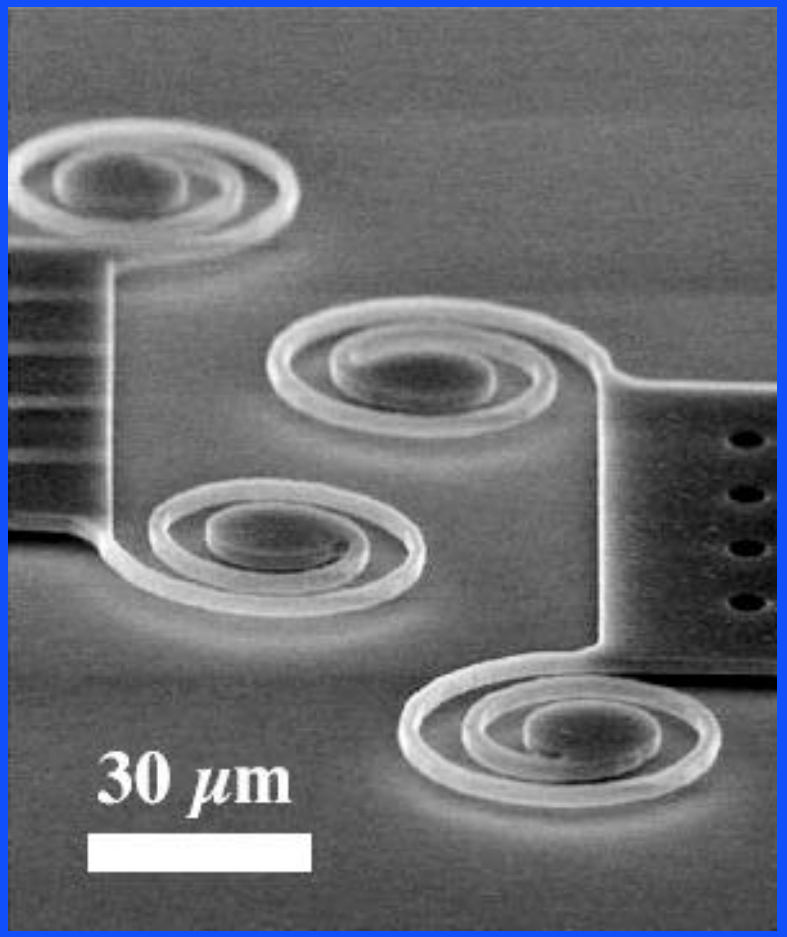
Fabricated using Microelectronics Center of North Carolina's MEMS Foundry Service.

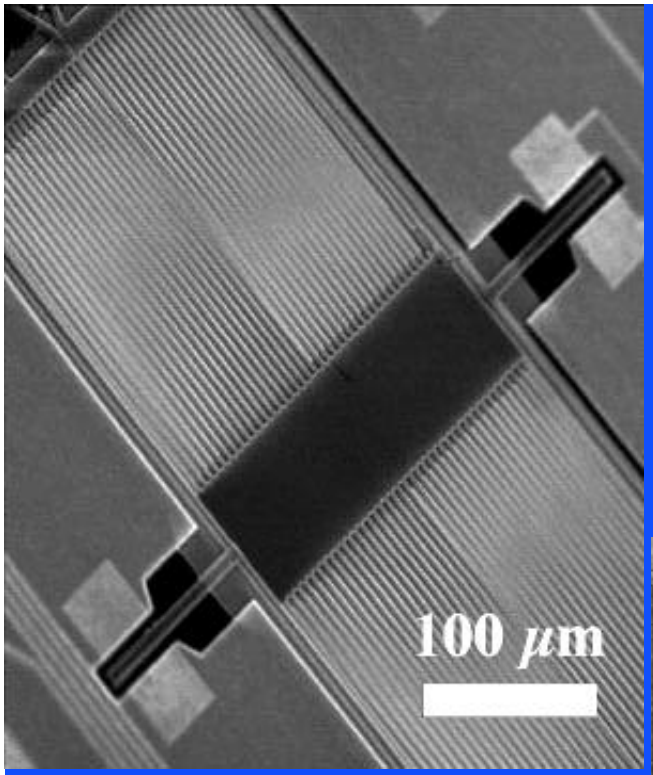


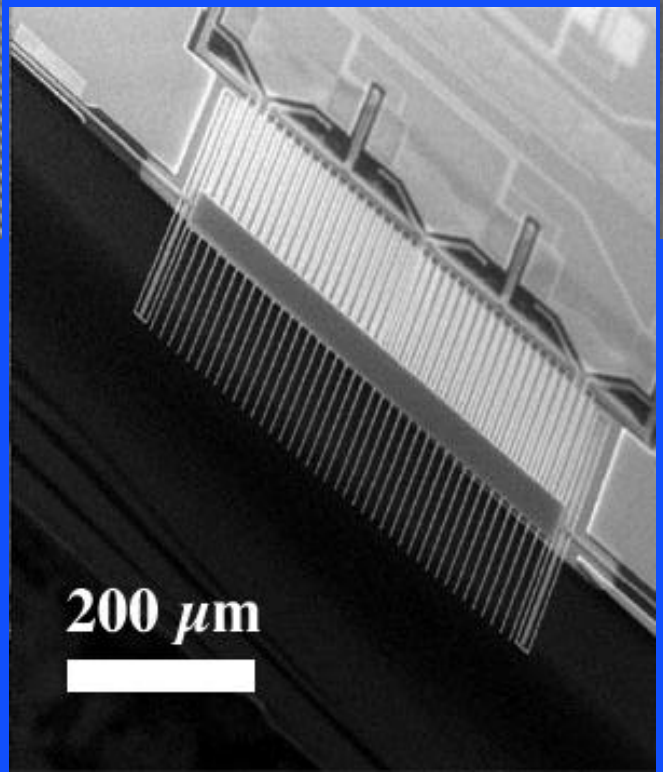
Courtesy Prof. A. Pisano, U. C. Berkeley.

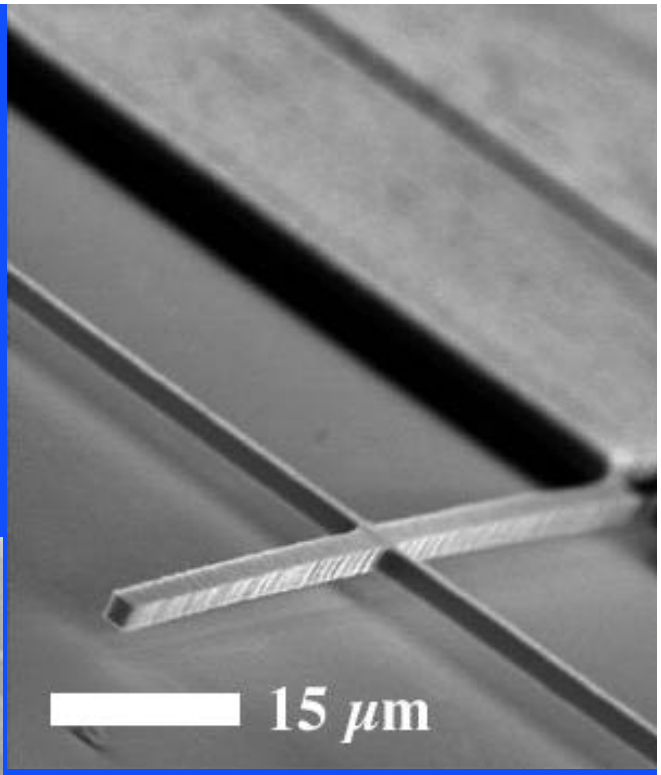
SPUTTERED Si DEVICES

- New sputtered-Si technology allows low-stress (and stress gradient) mechanisms.
- Low temperature deposition is CMOS compatible.
- Metal coating is feasible.
- Resonators, capacitors, and a number of other devices are possible.



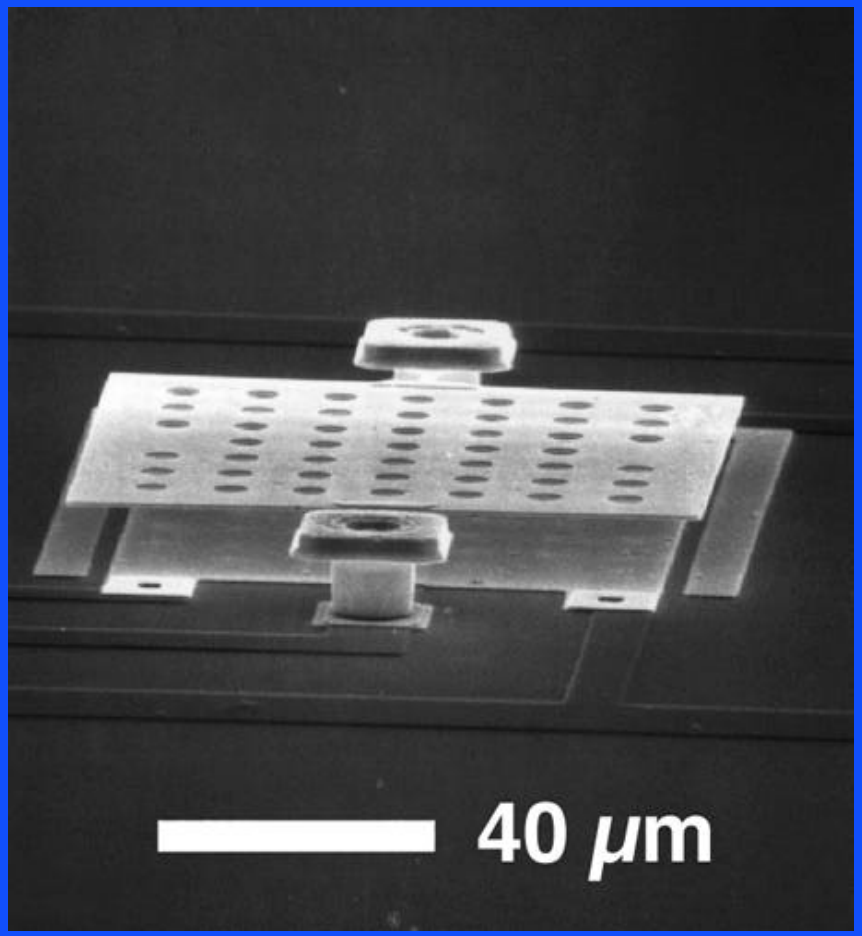


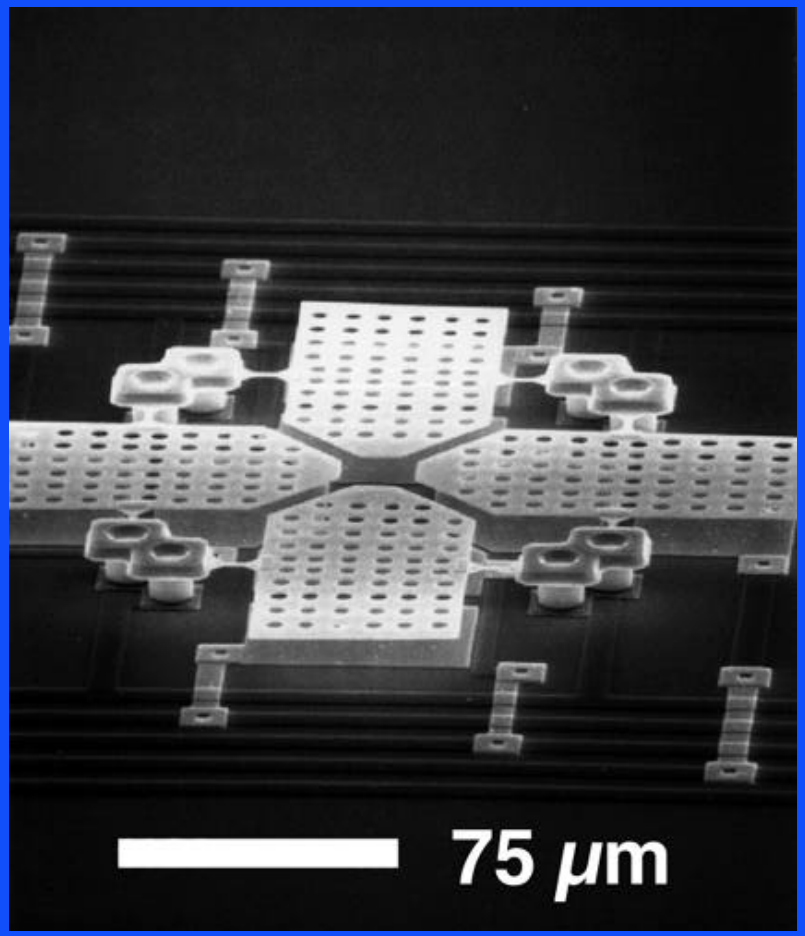




Reference: Honer, K.A. and Kovacs, G.T.A. "Sputtered silicon for microstructures and microcavities" Micro-Electro-Mechanical Systems (MEMS). 1999 International Mechanical Engineering Congress and Exposition. Held: Nashville, TN, USA 14-19 Nov. 1999

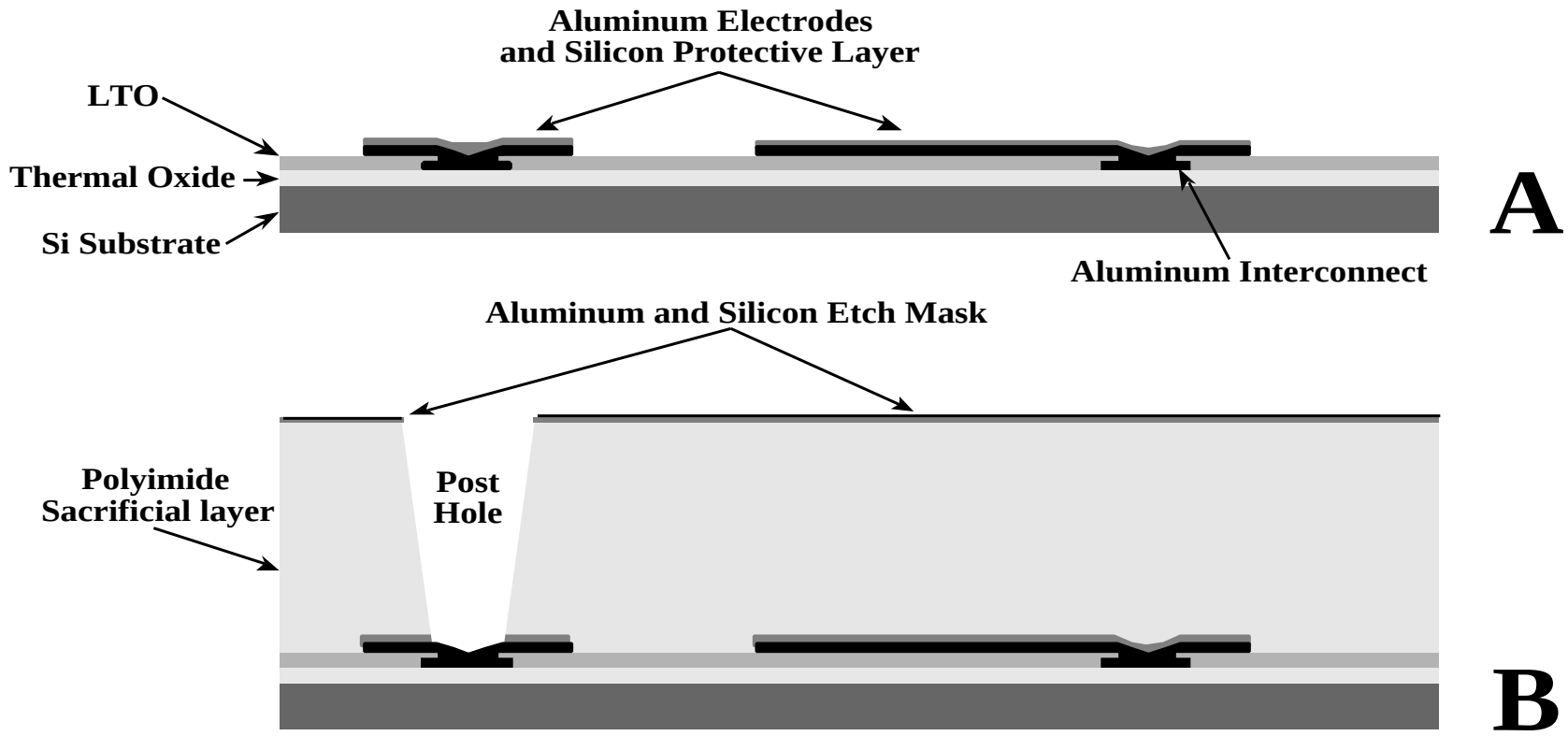
THIN-FILM ALUMINUM STRUCTURES

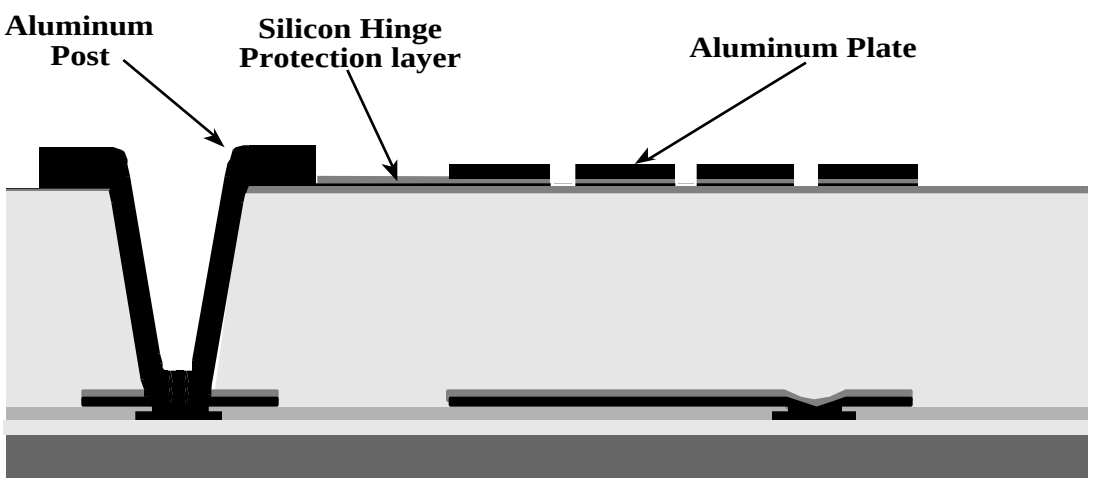


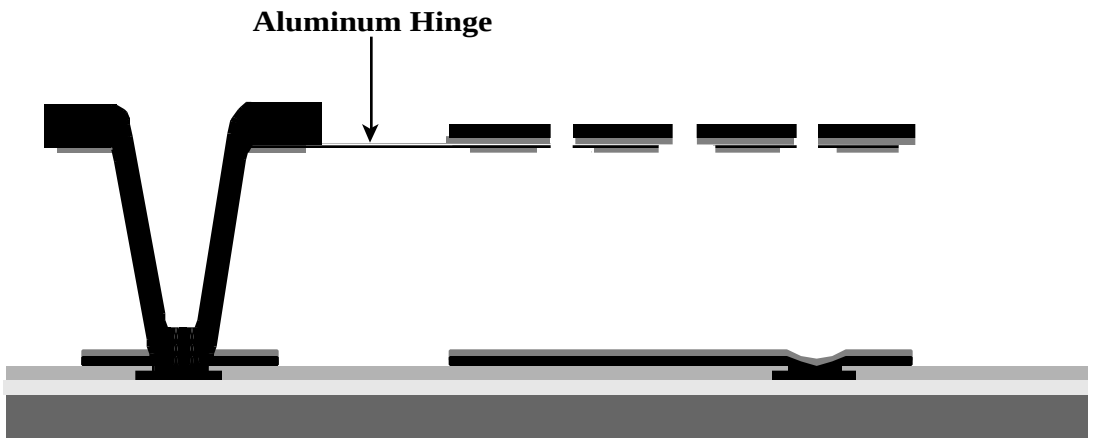


Reference: Storment, C. W., Borkholder, D. A., Westerlind, V., Suh, J. W., Maluf, N. I., and Kovacs, G. T. A., "Flexible, Dry-Released Process for Aluminum Electrostatic Actuators,"IEEE/ASME Journal of Microelectromechanical Systems, Sept. 1994, vol. 3, no. 3, pp. 90 - 96.

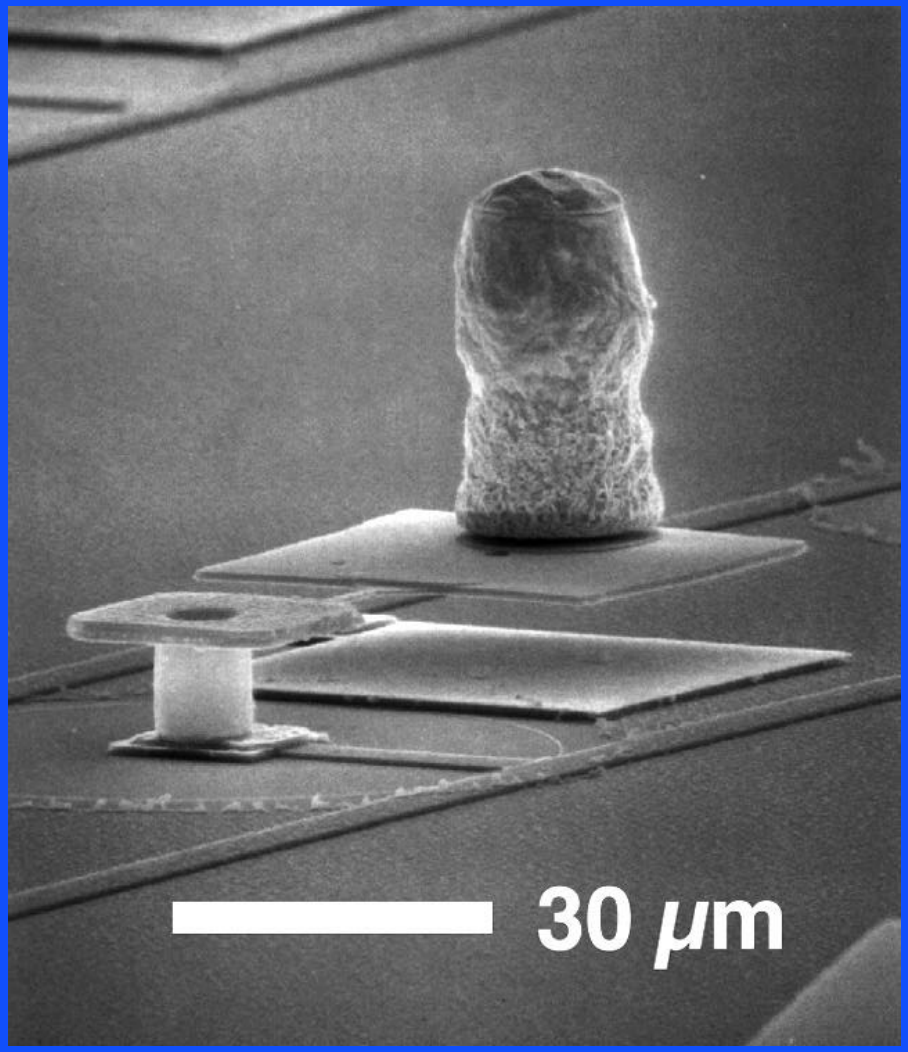
Al-MEMS Process Flow

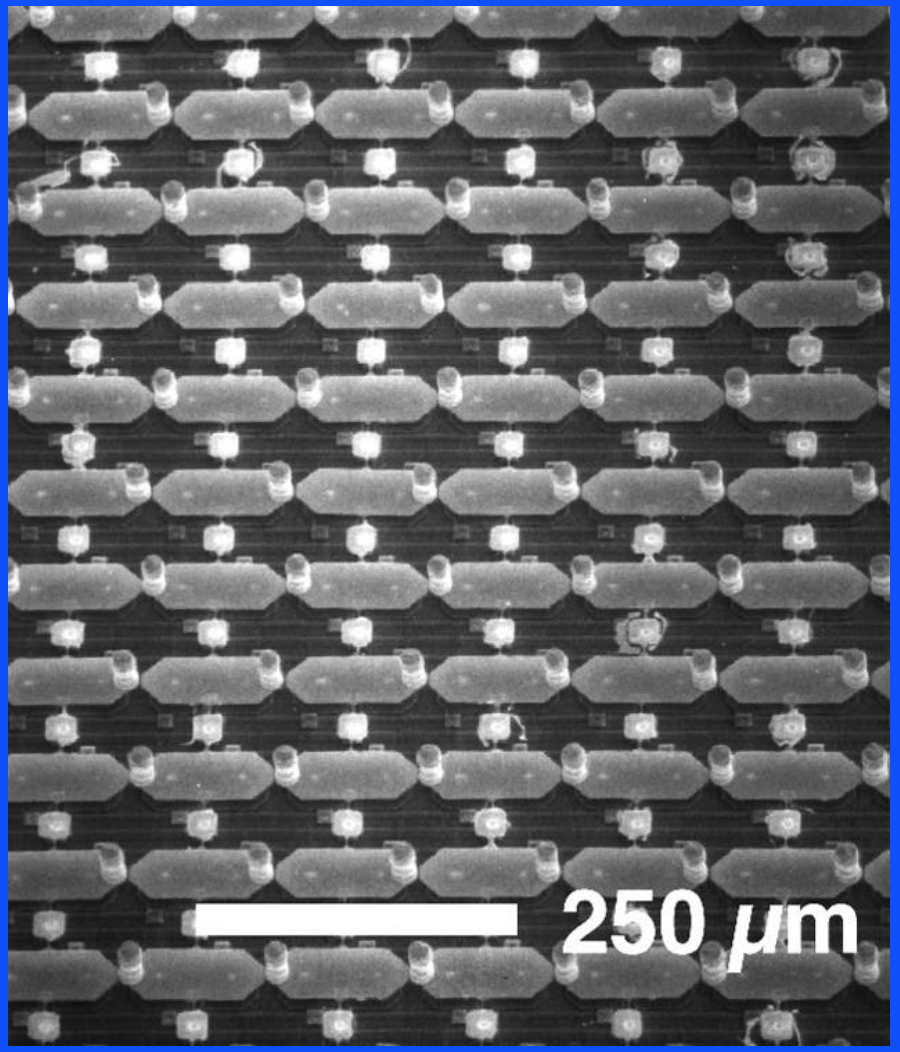






THIN-FILM + PLATING

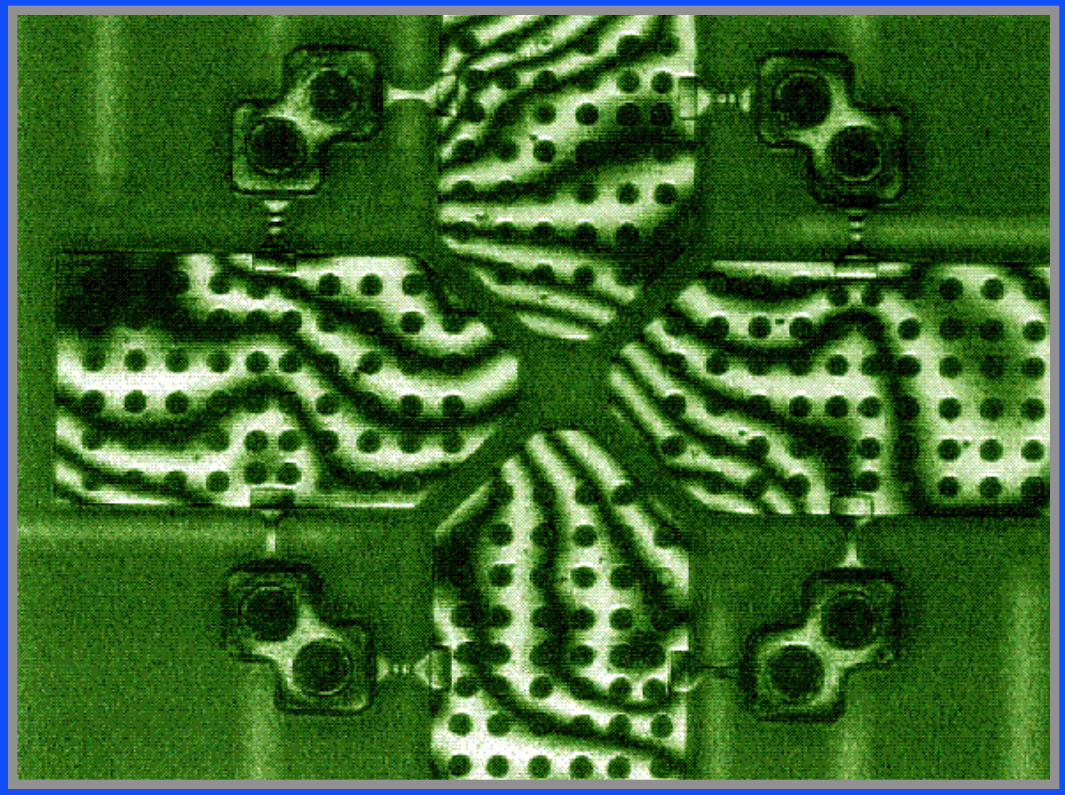




Reference: Storment, C. W., Borkholder, D. A., Westerlind, V., Suh, J. W., Maluf, N. I., and Kovacs, G. T. A., "Flexible, Dry-Released Process for Aluminum Electrostatic Actuators,"IEEE/ASME Journal of Microelectromechanical Systems, Sept. 1994, vol. 3, no. 3, pp. 90 - 96.

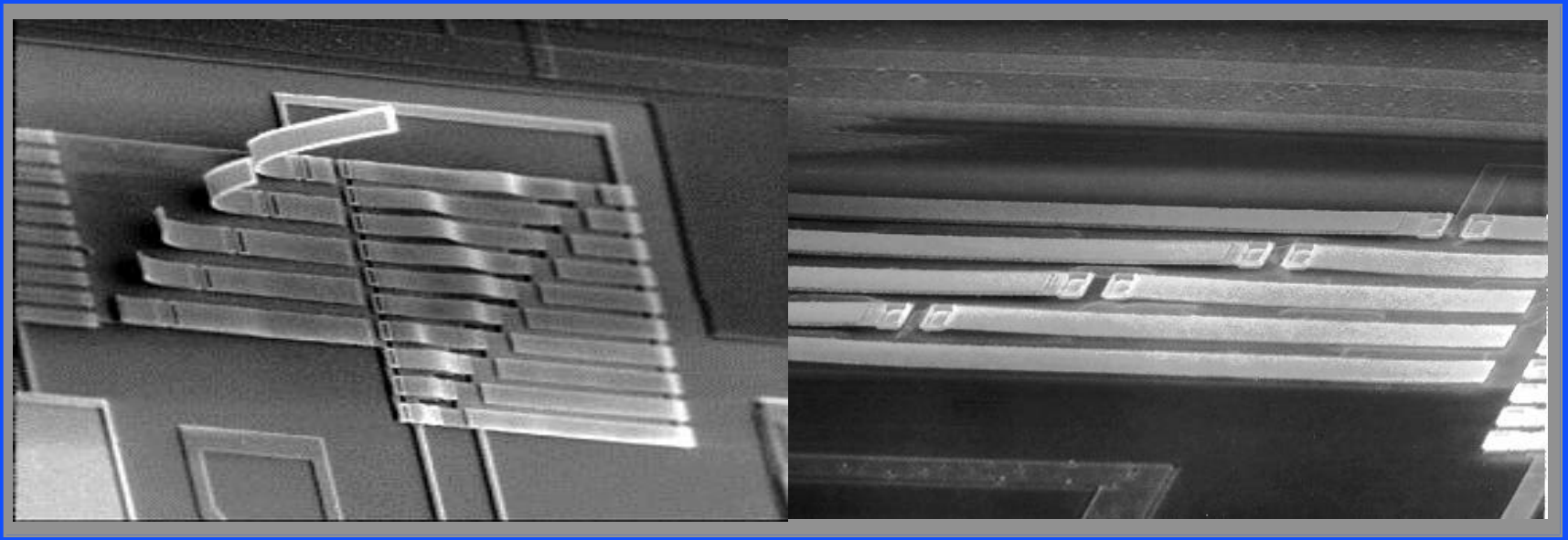
STRESS ISSUES IN THIN-FILM DEVICES

- **Stress gradients can have huge impact on the planarity of thin-film microstructures.**
- **Such gradients may be “as deposited,” or induced by the release process, particularly if it is energetic (such as a plasma release).**



Interference microscopy courtesy Mr. P. Congdon, Texas Instruments, Inc.

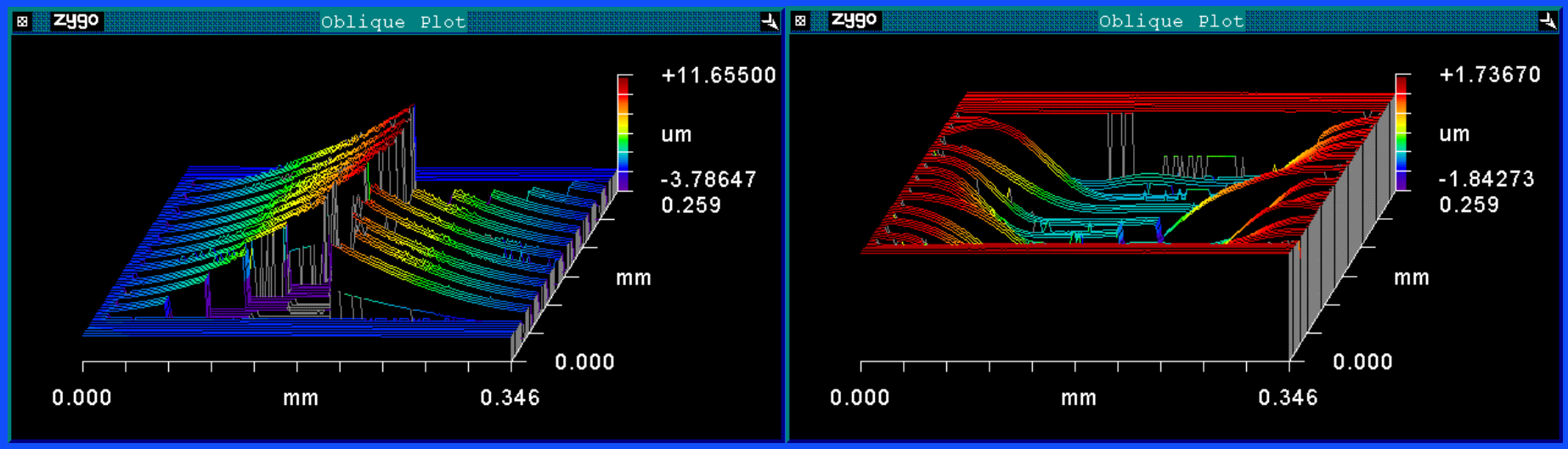
EFFECTS OF RELEASE METHOD



SF_6 Plasma versus XeF_2

Courtesy Ken Honer, Stanford University.

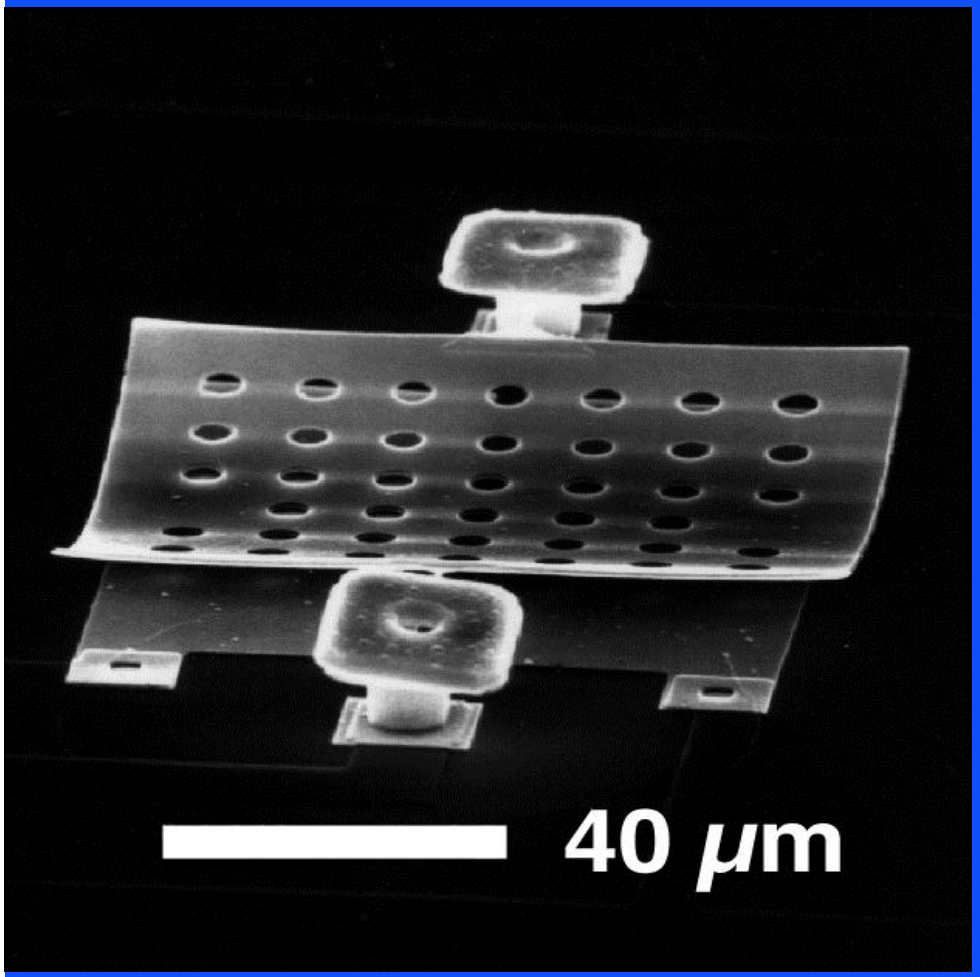
EFFECTS OF PLASMA POWER

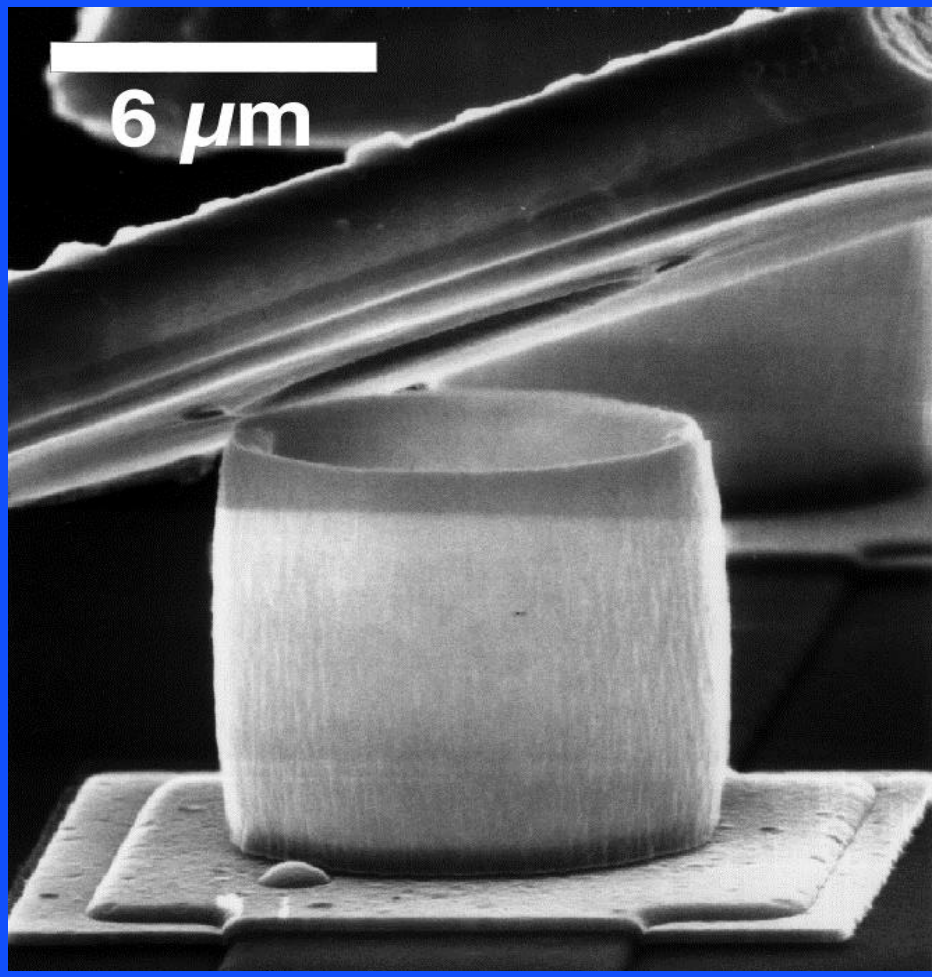


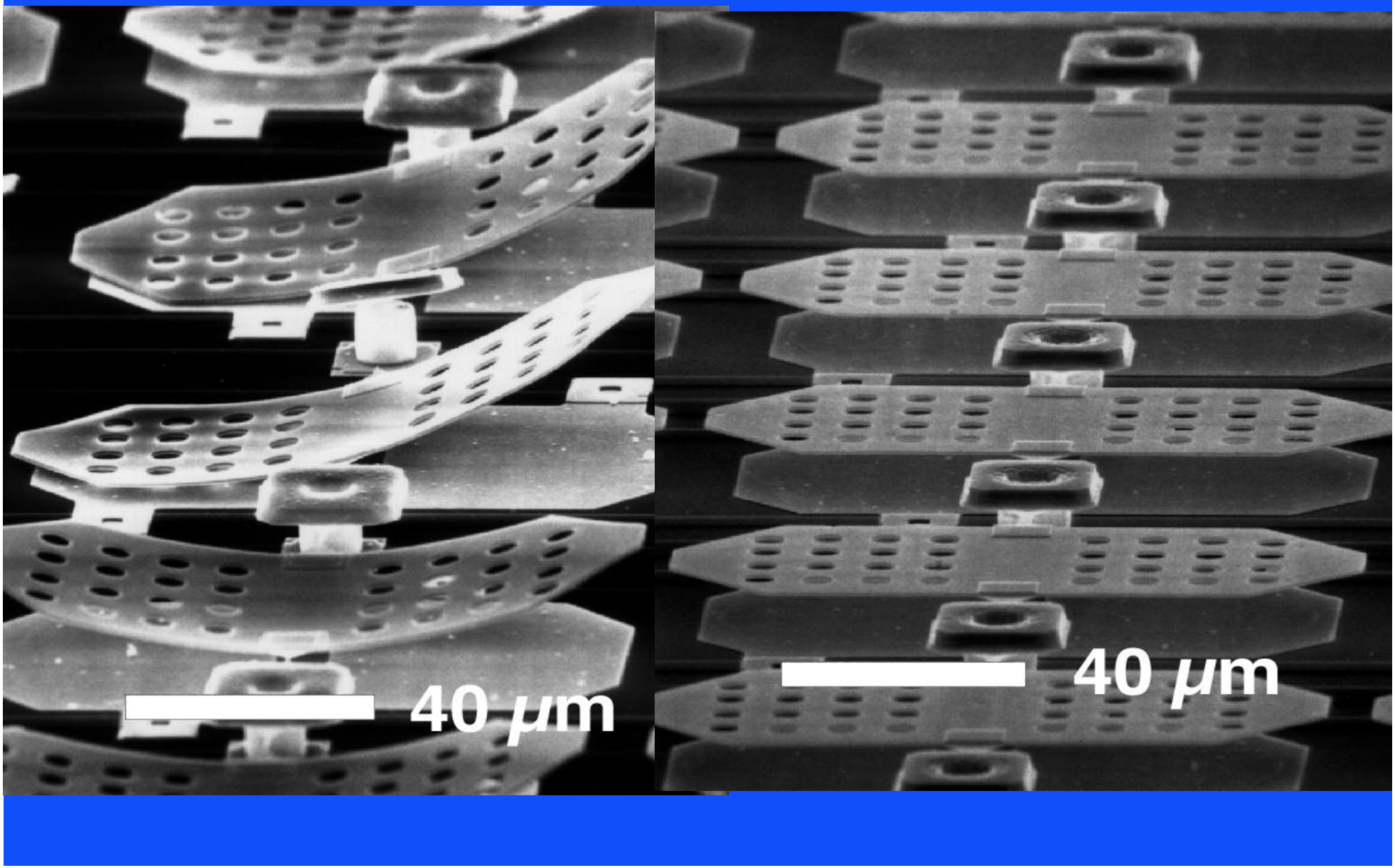
200W Vs. 50W

Courtesy Ken Honer, Stanford University.

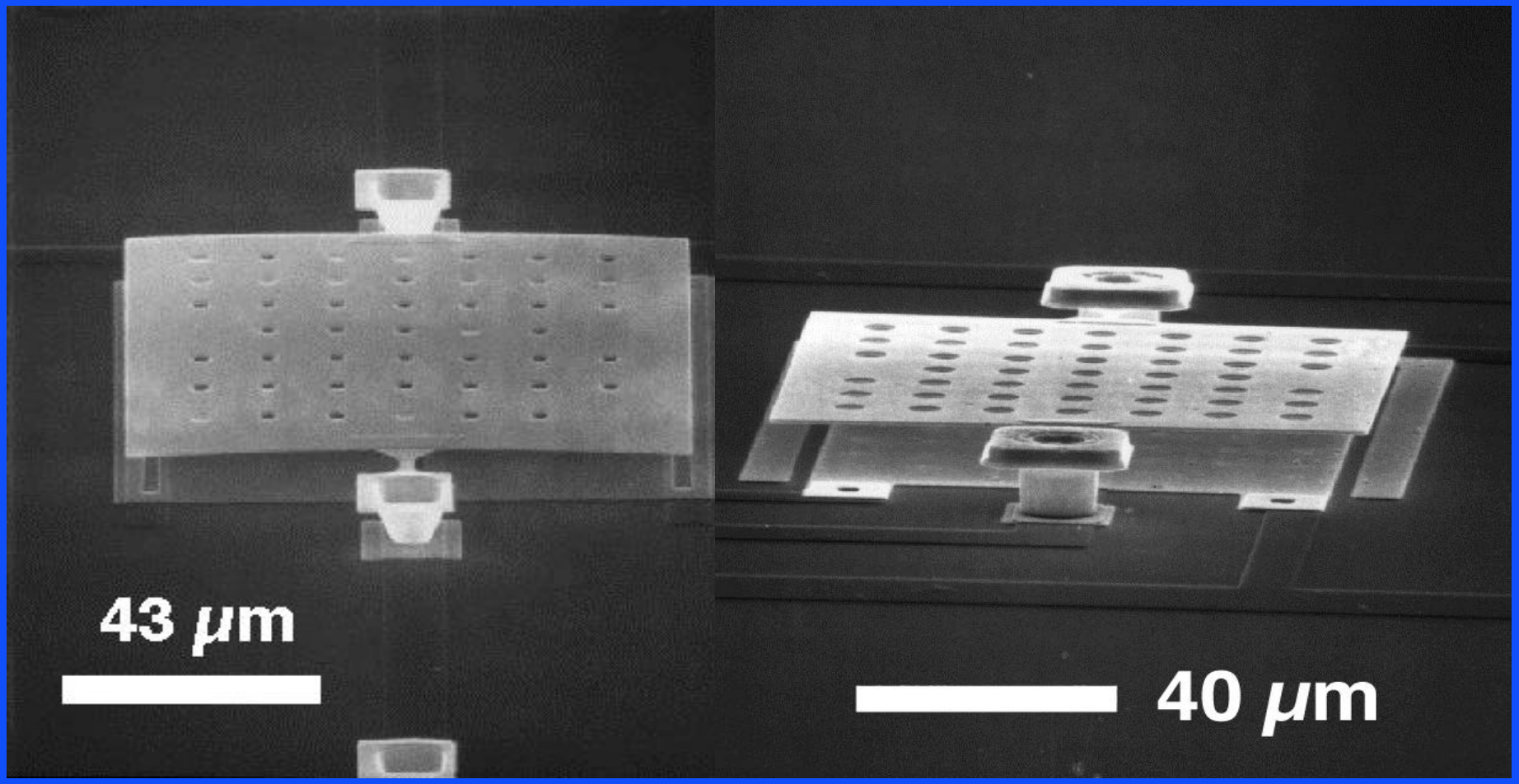
CAN YOU SAY STRESS?



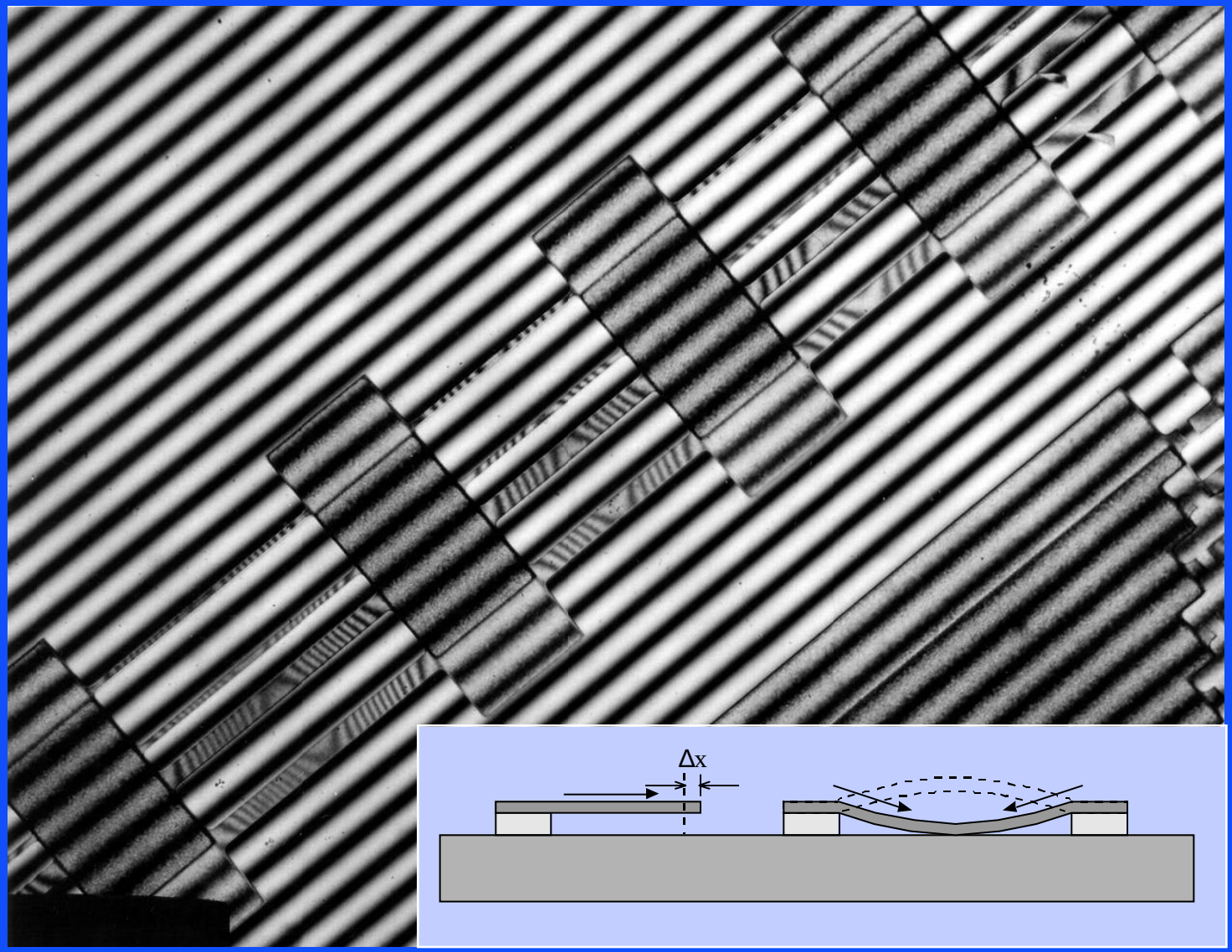



40 μm
40 μm

IMPROVED TORSIONAL DESIGNS

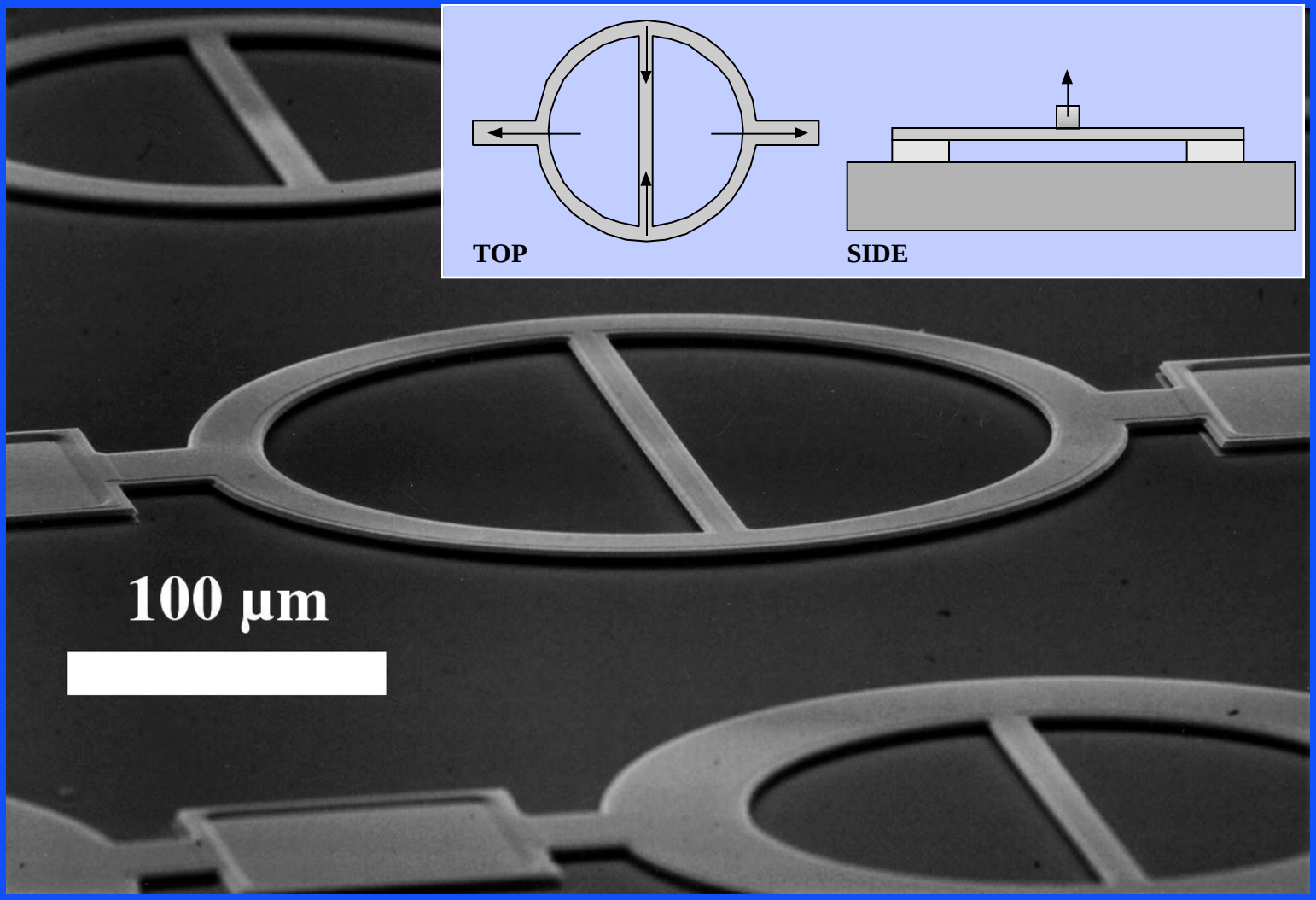


INTERFERENCE MICROSCOPY OF BEAMS



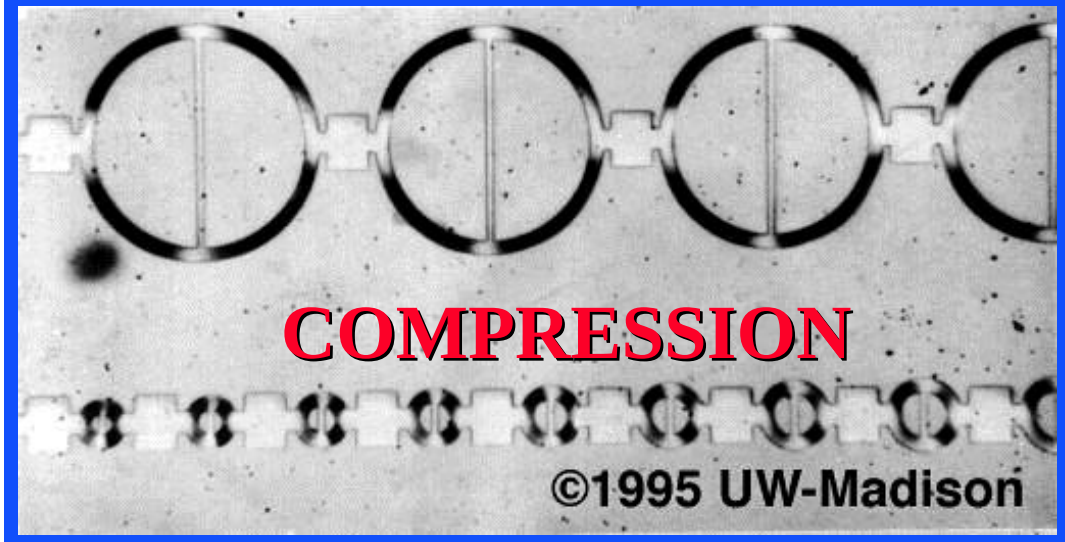
Courtesy Dr.
L. Ristic,
Motorola, Inc.

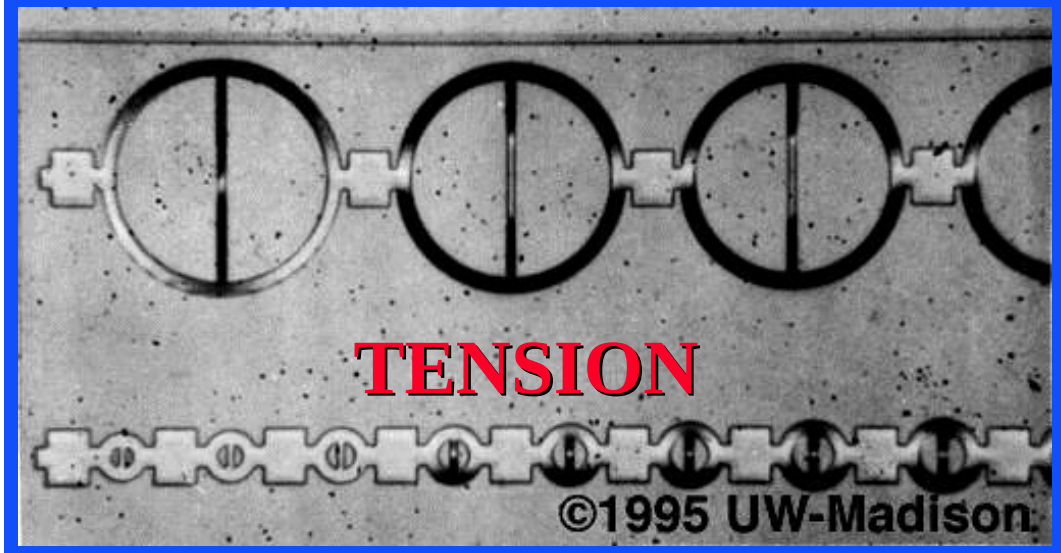
GUCKEL RINGS

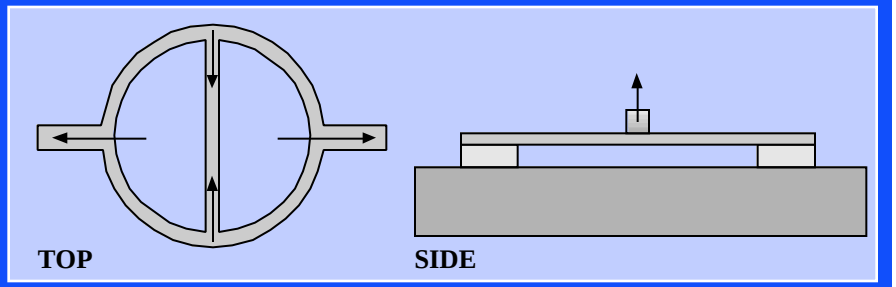


Courtesy Dr. L. Ristic, Motorola, Inc.

GUCKEL RINGS

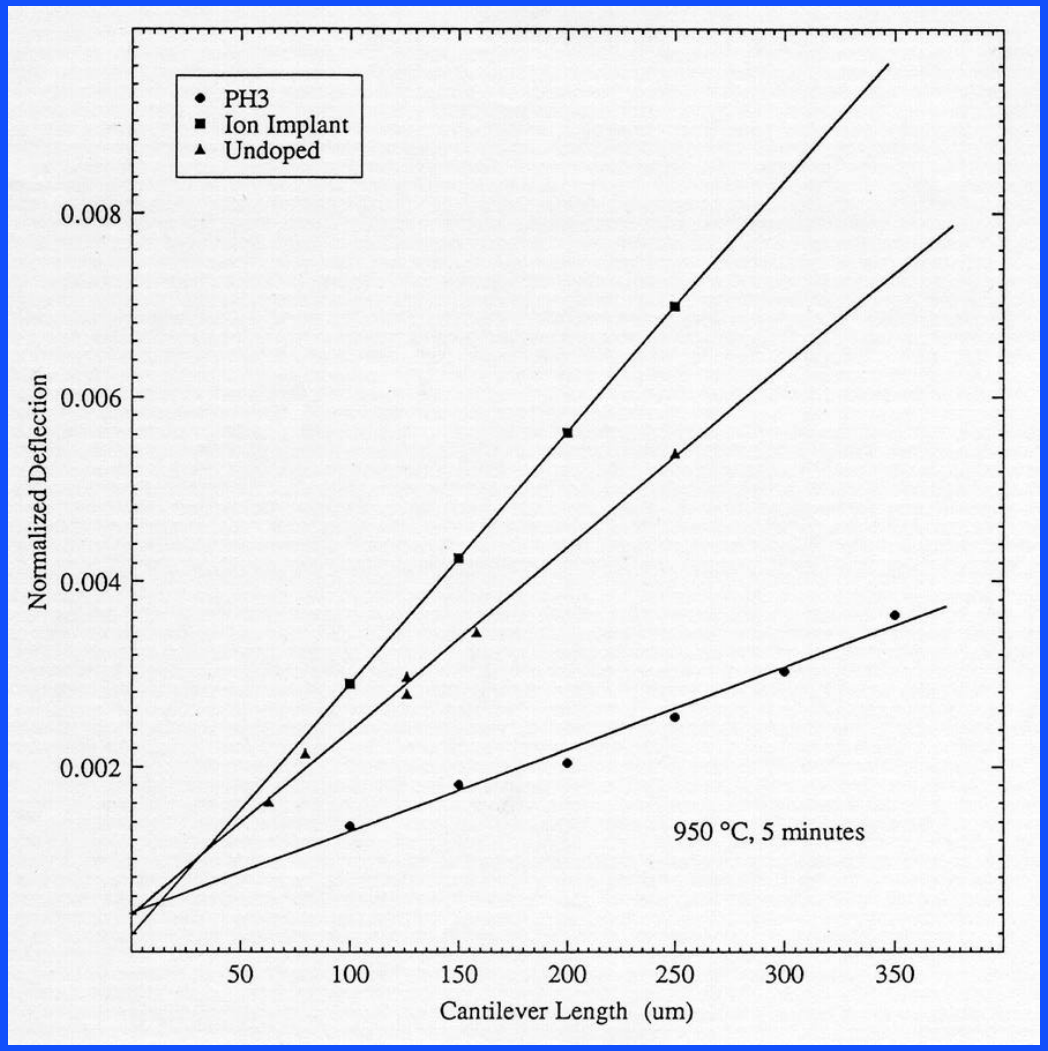






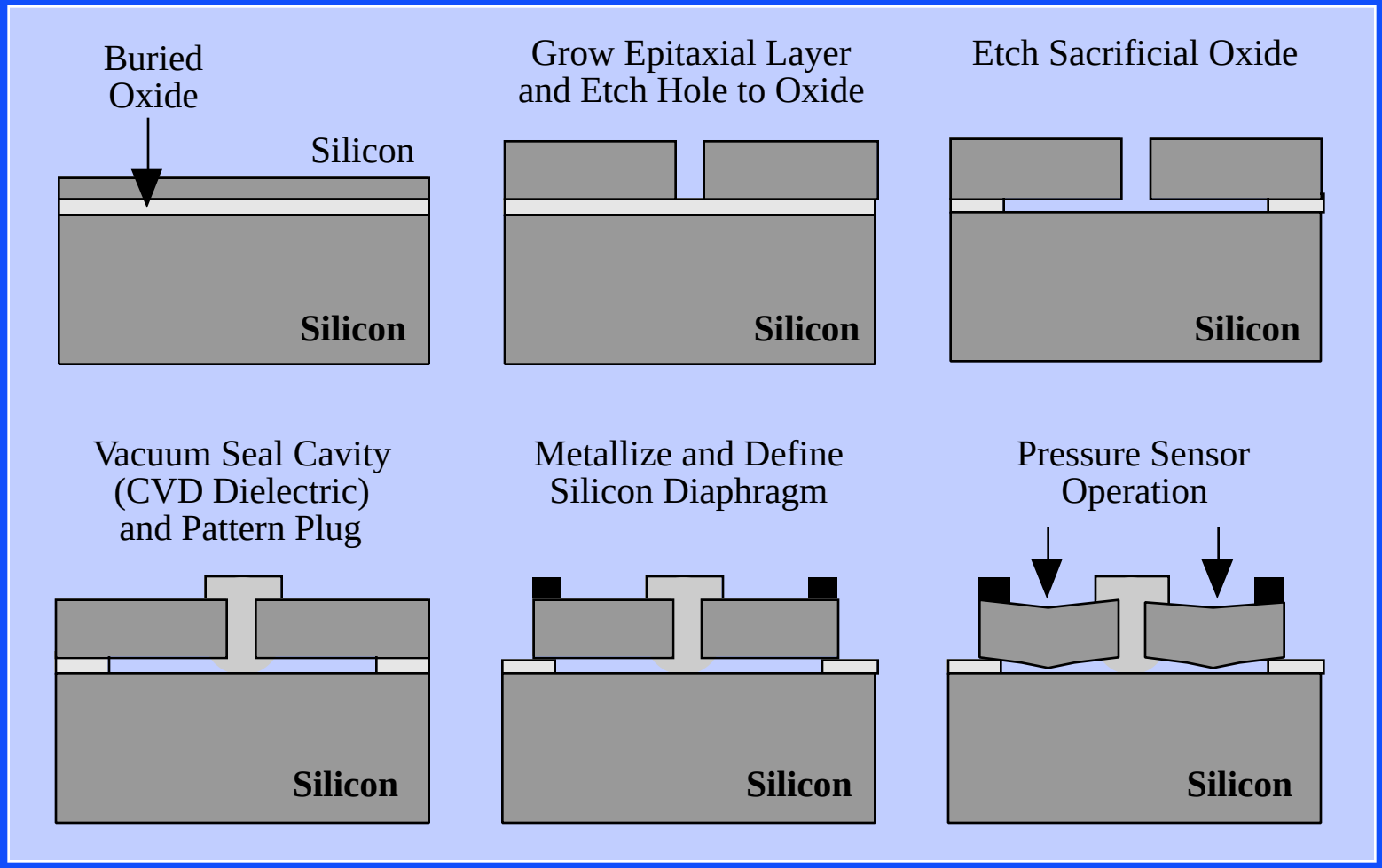
Images courtesy Prof. H. Guckel, University of Wisconsin.

EFFECTS OF ANNEALING ON POLYSILICON STRESS GRADIENTS

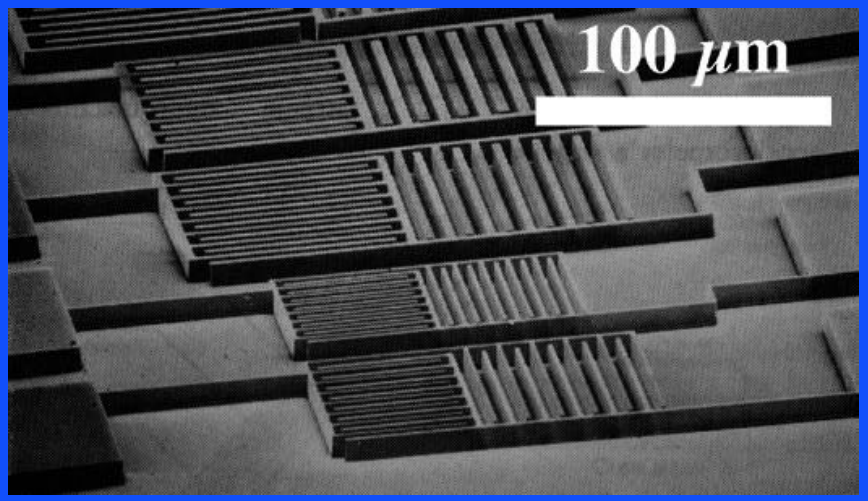


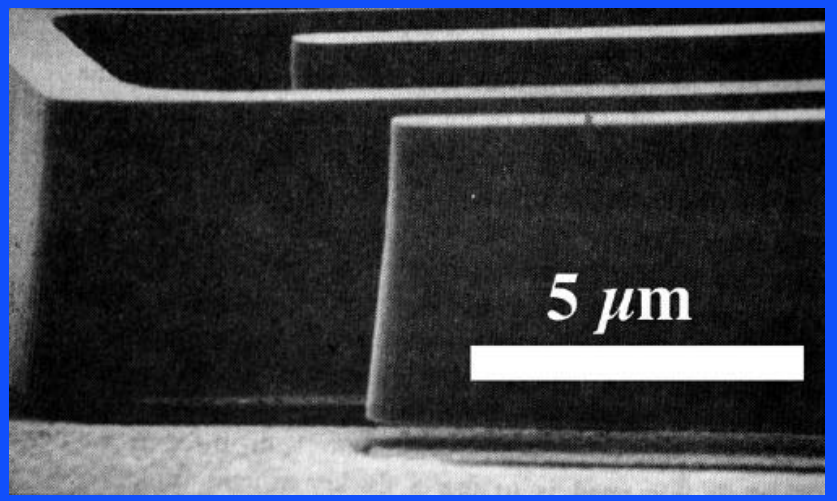
Courtesy Dr. L. Ristic, Motorola, Inc.

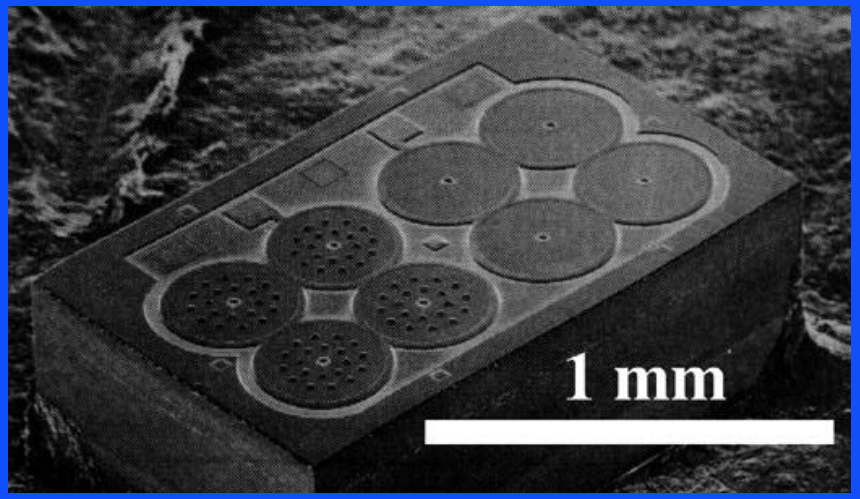
SIMOX AS A SACRIFICIAL LAYER

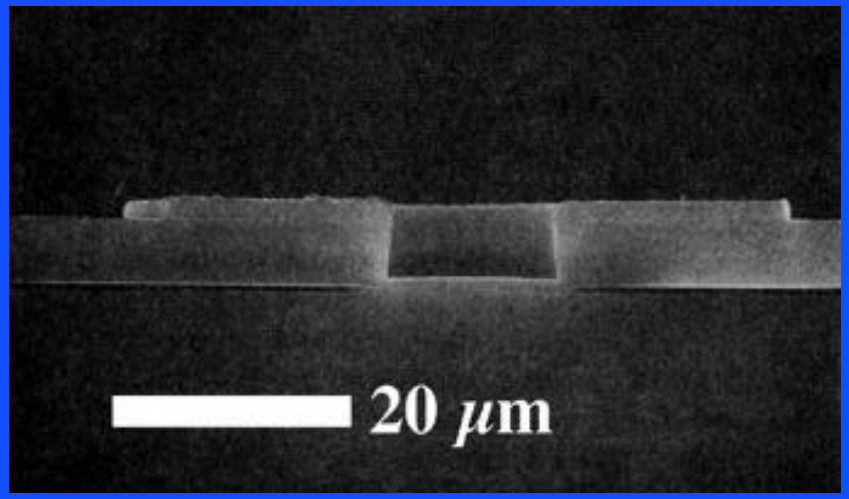


Sacrificial SIMOX sealed-cavity pressure sensor fabrication, after Diem, et al., (1993).









Source: Diem, B., Delaye, M. T., Michel, F., Renard, S., and Delapierre, G., "SOI (SIMOX) as a Substrate for Surface Micromachining of Single Crystalline Sensors and Actuators," Proceedings of Transducers '93, the 7th International Conference on Solid-State Sensors and Actuators, Yokohama, Japan, June 7 - 10, 1993, Institute of Electrical Engineers, Japan, pp. 233 - 236.

TEMPLATE REPLICATION

Microtool fabrication by etch pit replication

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(Received 13 August 1973; and in final form , 30 August 1973)

Small tools can be made by etching one of a variety of crystallographically limited pits into a single crystal mandrel, filling the pit with tool material and removing the mandrel. Fabrication of arrays of chisels and pyramidal points using a silicon mandrel and process technology common in the semiconductor electronics industry is discussed.

I. INTRODUCTION

Some microtools, such as scribes and chisels used for ruling optical gratings, are made from single crystal diamond or sapphire chips that are individually ground to shape. Others, such as integrated circuit bonding wedges, are partially made by powder metallurgy techniques and are finished by grinding.

An alternative method of making small tools of a variety of crystallographically limited shapes is to etch a pit into a single crystal mandrel, fill the pit with a suitable tool material, attach the tool (or array of tools) to suitable mounts, and then to remove the mandrel. This procedure permits the fabrication of very small tools, the ultimate sizes of which are limited to micron or submicron dimensions by photo or electronlithographic precision. Batch fabrication of arrays in which the positions of the individual elements are set with respect to each other with the same precision is also possible.

II. TOOL FABRICATION

For many uses, the ready availability of the material and the sophistication of the associated microelectronic technology recommend the use of single crystal silicon wafers as the mandrel for this fabrication method. Wafers with a (100) crystalline orientation [preferably with a (110) flat] are commonly employed in MOS device fabrication, and can be adapted to the formation of knife edges or pyramidal points. Chisel pointed tools, as will be discussed later, can be made from the somewhat less common (110) orientation. There are indications that this and other orientations [e.g. (112) and (115)] will become more readily available to exploit their special etching properties which permit the fabrication of a variety of dielectric-isolated circuit structures, but the best present approach to obtain (110) wafers is to saw them from a {111} ingot with a (11$\bar{2}$) flat.[1]

Prior to the formation of the etch pits, a suitable etch mask must be formed on the surface of the mandrel and used to delineate the desired pit geometry. If the mandrel is silicon, one can use a thermally grown SiO_2 film to mask against the subsequent silicon etching, and delineate a pattern in the SiO_2 mask by well-known photolithographic techniques.[2] Contemporary photolithographic precision permits one to fabricate micron-sized pits and to control interpit spacing to comparable tolerances across a 5 cm wafer. Recent developments in electronlithography indicate that 0.1 μ precision is to be expected in both size and interpit spacing within a few years.[3]

The pits, once delineated, are etched with a crystallographically selective etchant. In the case of silicon, a variety of etchants[4–6] is available that etch the most densely packed {111} planes slowest and that are compatible with an SiO_2 etch mask. Since the etch pits will be bounded by several of the slowest etching planes, the figures that can be employed are limited to those that can have their edges aligned parallel to the intersections of {111} planes with the plane of the mandrel. For a (100) wafer, this implies that the mask figures may be either squares or rectangles that are set so that their edges are parallel to the two ⟨110⟩ directions in which the {111}'s intersect (100), as is shown in Fig. 1. If a (110) mandrel is employed, the mask figure must be either a rhombus or a parallelogram in which one of the internal angles is 70.53°. These figures are aligned with the ⟨112⟩ directions along which four {111}'s intersect (110), as indicated in Fig. 2.

The ratio of the pit's depth to its width is limited by crystallographic considerations. For the (100) silicon mandrel, for example, the depth limiting {111}'s aligned with the mask intersect (100) at 54.74° and limit the pit depth to about 0.7 of the minimum side of the mask square or rectangle. For the (110) mandrel, on the other hand, the sides of the etch figure are aligned with four {111}'s that are perpendicular to (110) and the depth limit is set by two other {111}'s that intersect (110) along ⟨110⟩ directions at 35.26°. In this case the depth is limited to about 0.35 of

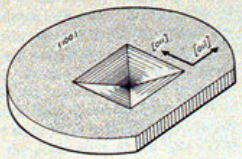


FIG. 1. (100) wafer orientation showing intersection of {111}'s along ⟨110⟩.

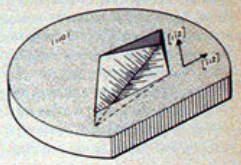
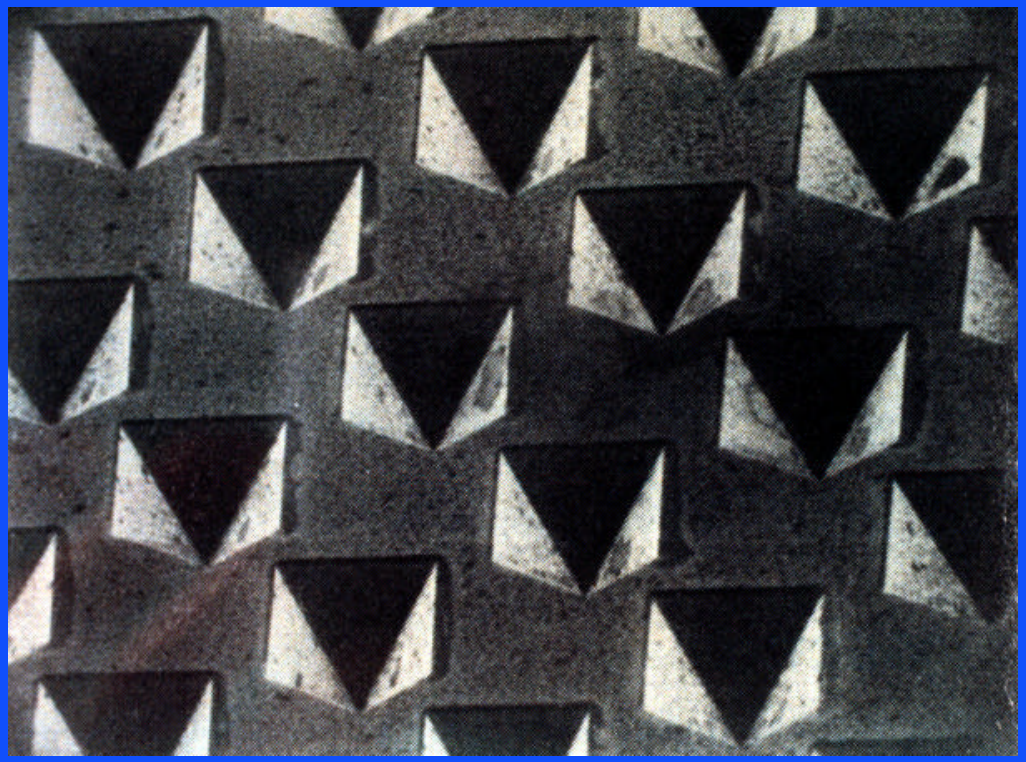


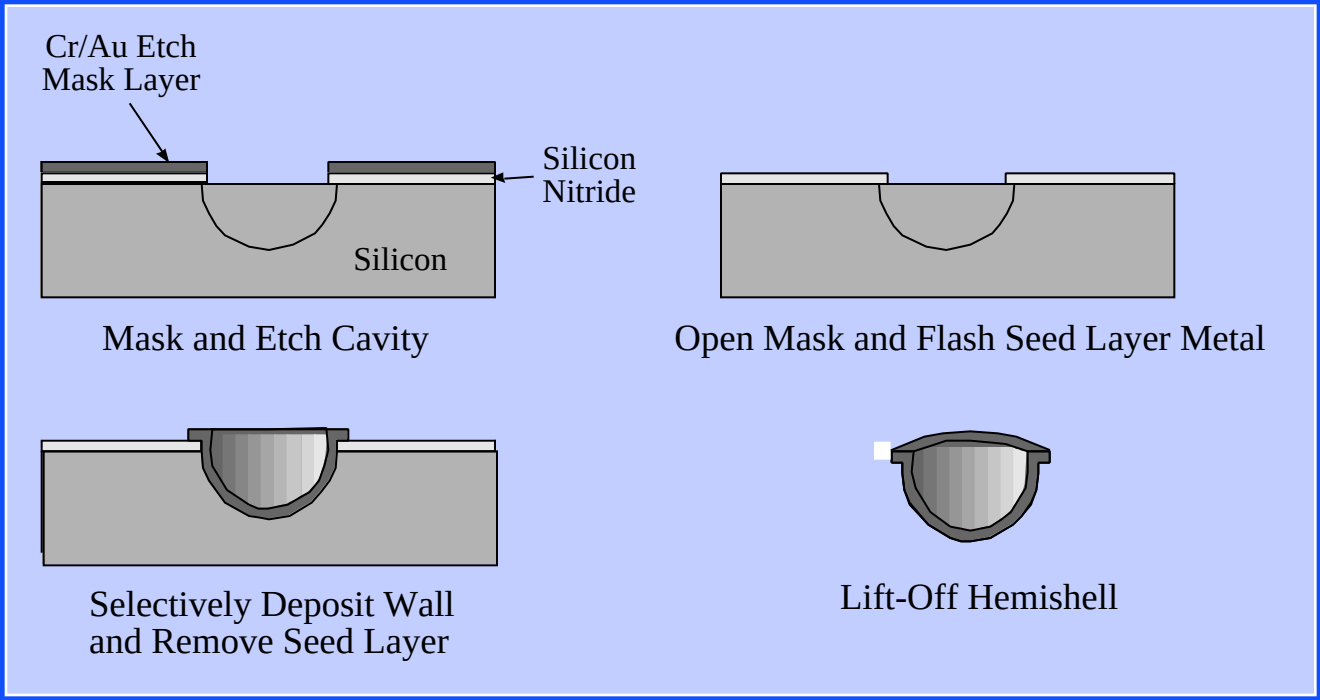
FIG. 2. (110) wafer orientation showing intersection of {111}'s along ⟨112⟩ and ⟨110⟩.



Source: Kiewit, D. A., "Microtool Fabrication by Etch Pit Replication," Review of Scientific Instruments, vol. 44, no. 12, Dec. 1973, pp. 1741 - 1742.

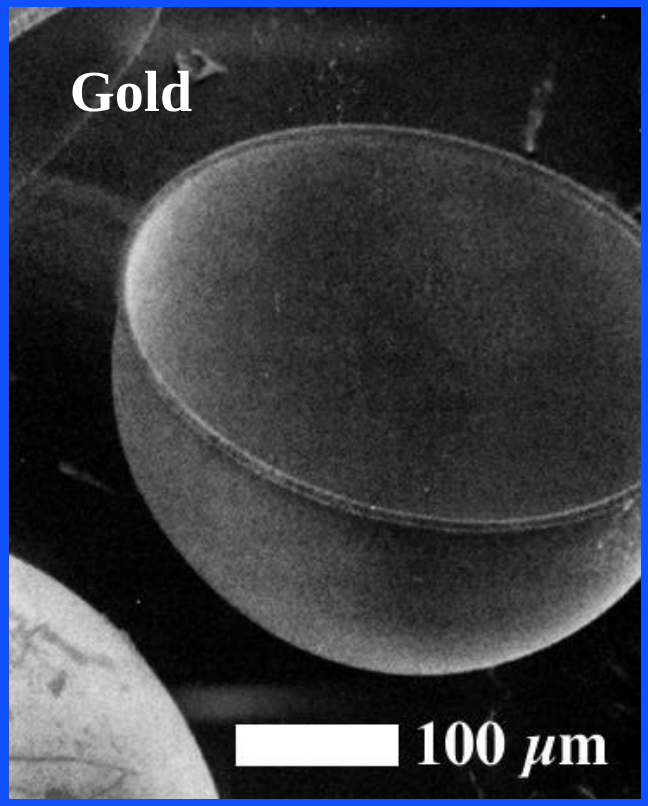
TEMPLATE REPLICATION

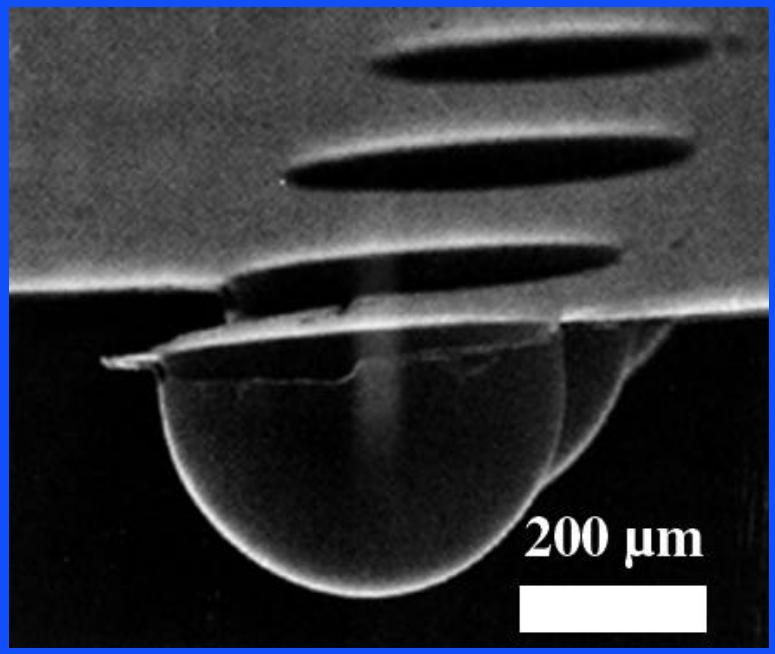
- **Template replication (etching a pit and depositing a film into it to replicate the shape) can be used for a variety of structures.**



Fabrication sequence for free-standing metal hemishells using an isotropic silicon-etching technique. (After Wise, et al., (1979 and 1981).)

HEMISHELL FABRICATION





Silicon Dioxide (5 μm thick)

From Wise, et al., (1979 and 1981).

CVD-BASED TEMPLATE REPLICATION

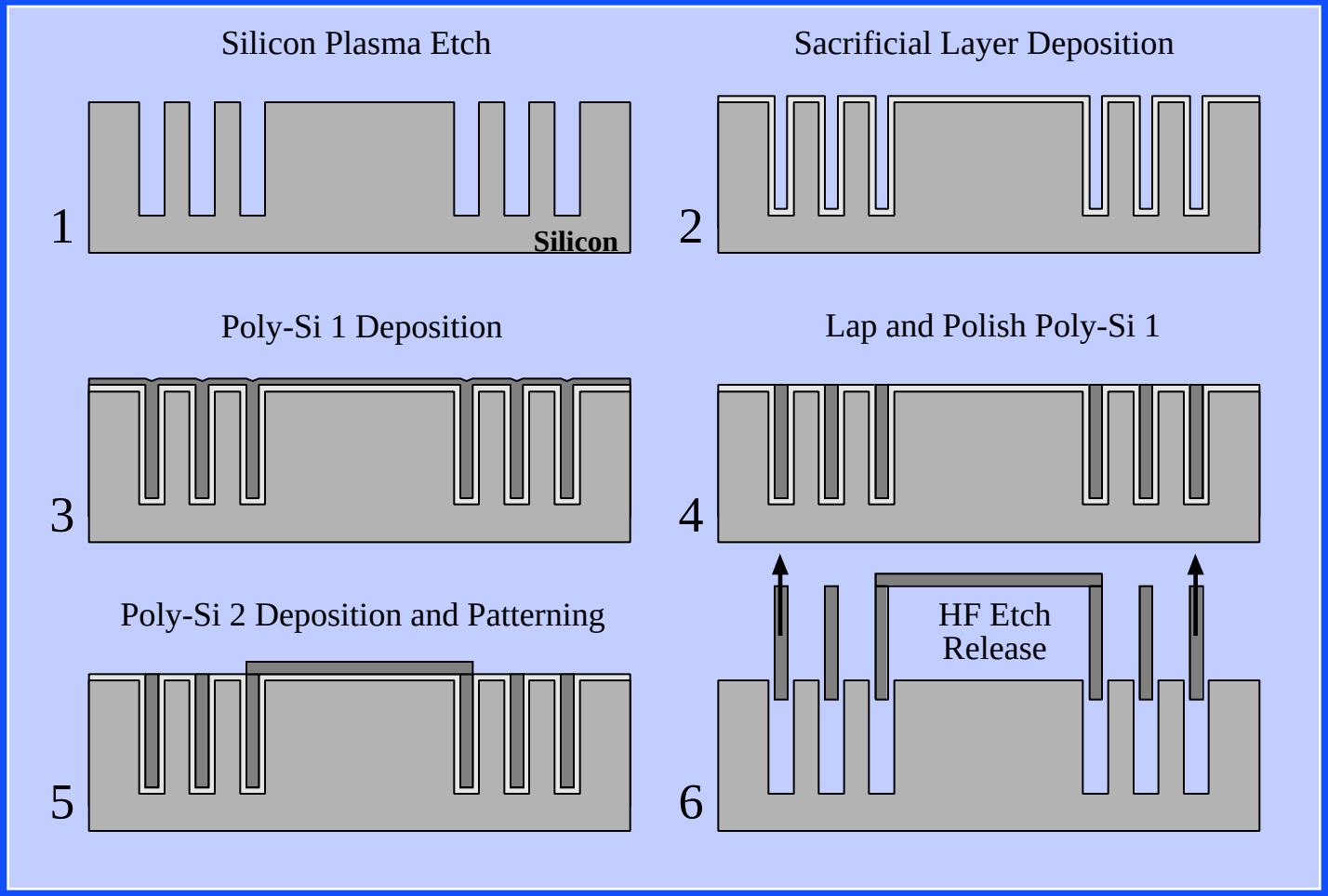
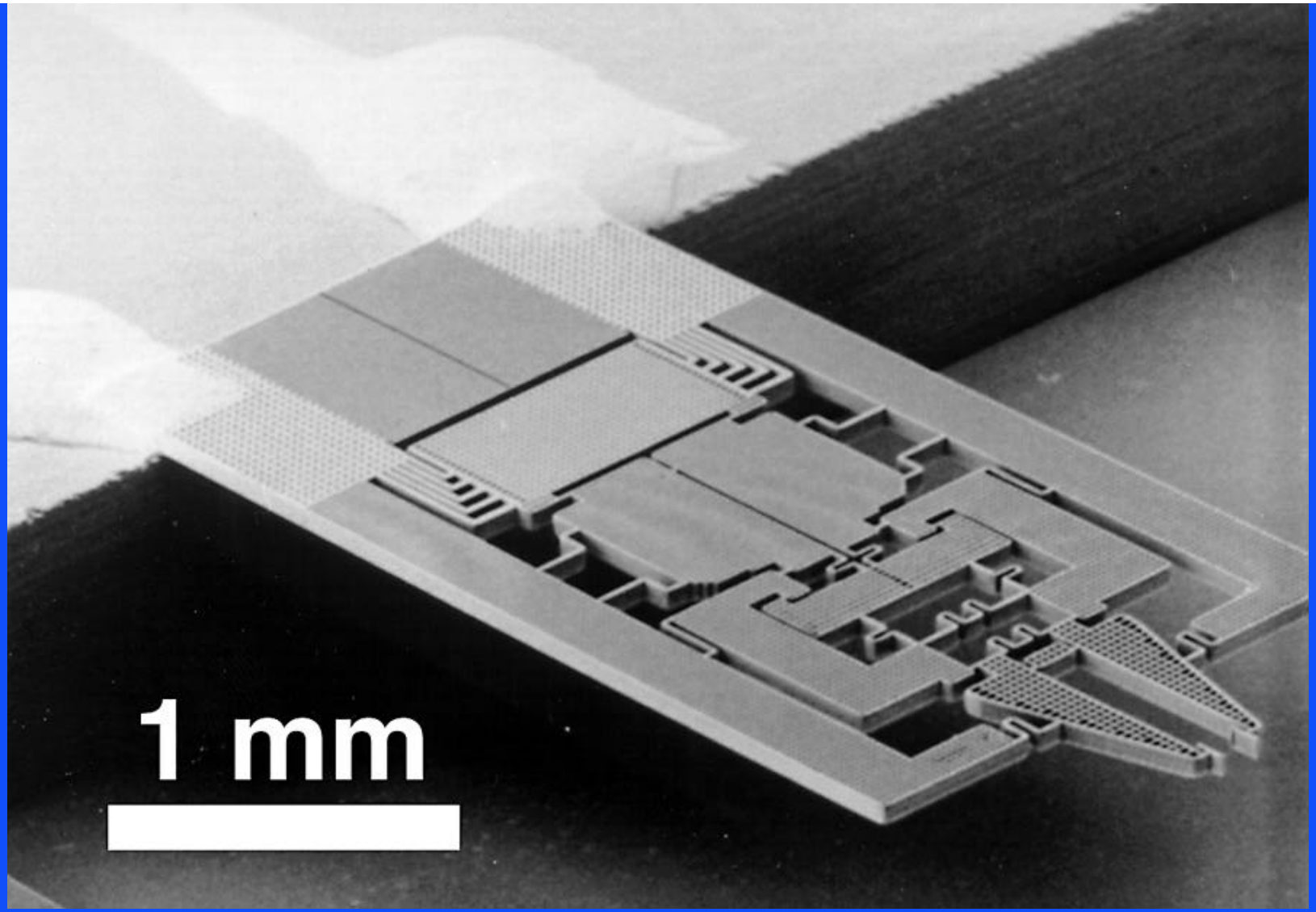
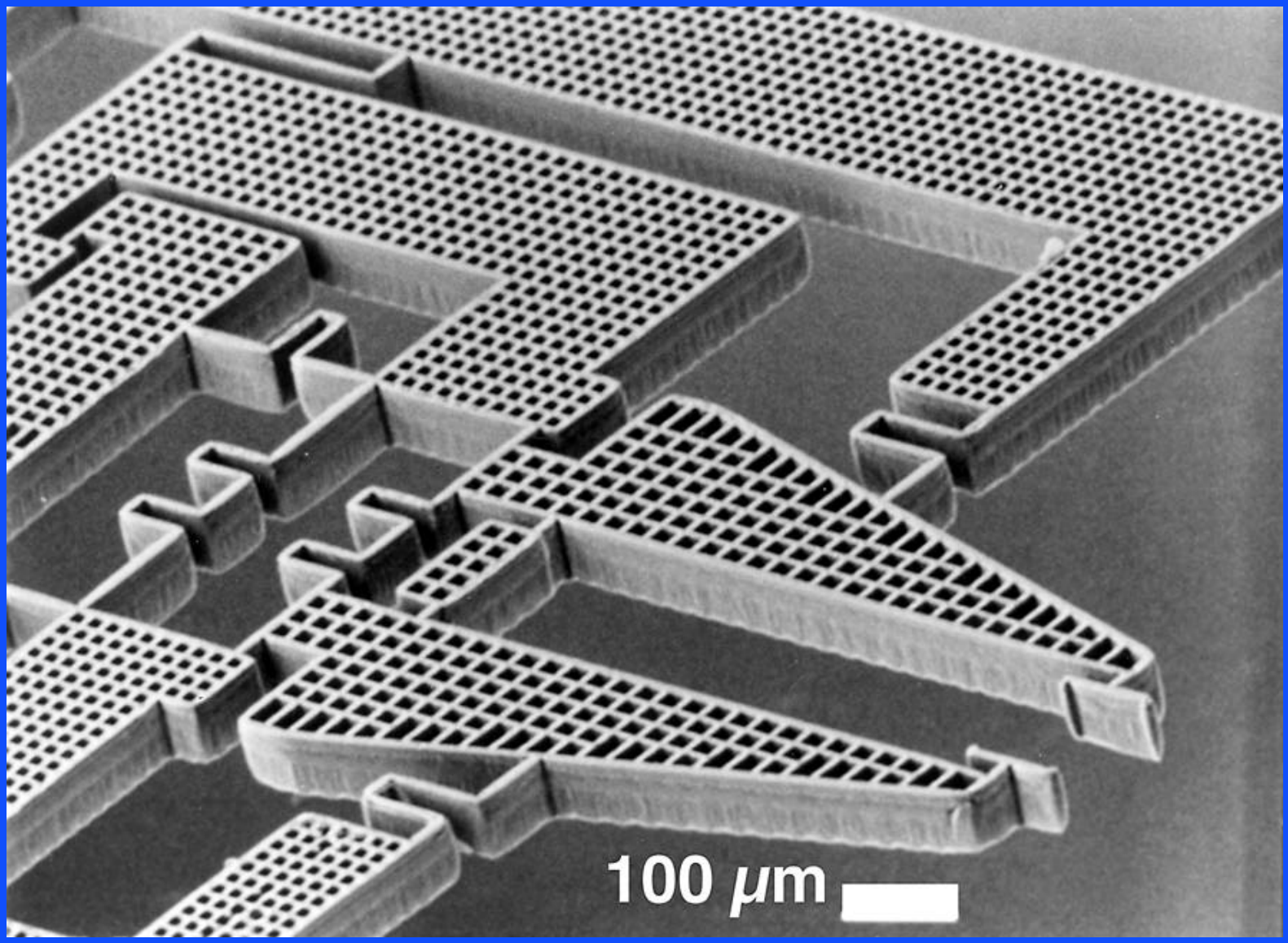


Illustration of template-molded polysilicon process, after Keller and Ferrari (1994).

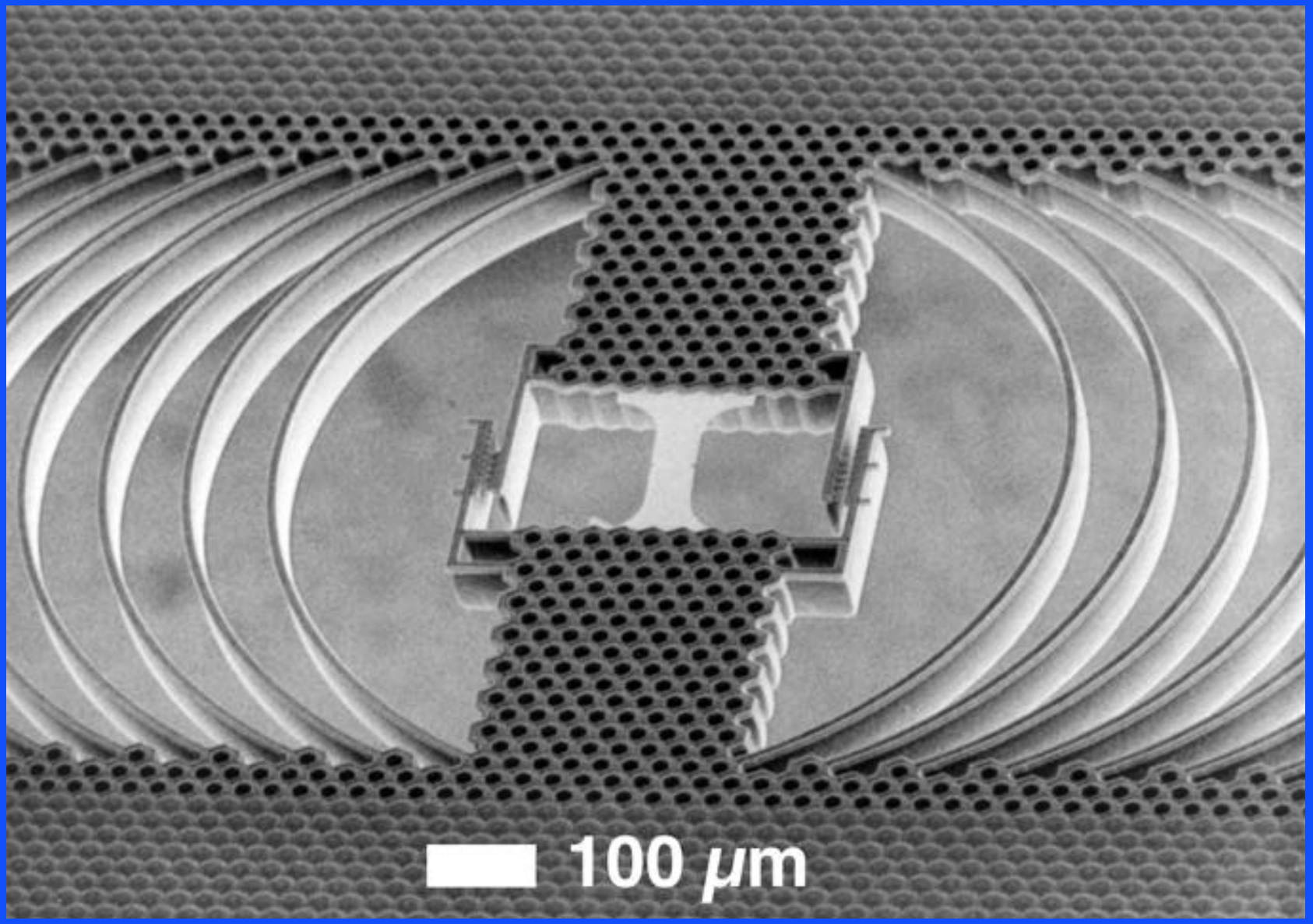


Courtesy of Chris Keller, U. C. Berkeley.

Reference: Keller, C. G., and Howe, R. T., "Hexsil Bimorphs for Vertical Actuation," Proceedings of Transducers '95, the 8th International Conference on Solid-State Sensors and Actuators, Stockholm, Sweden, June 25 - 29, 1995, vol. 1, pp. 99 - 102.

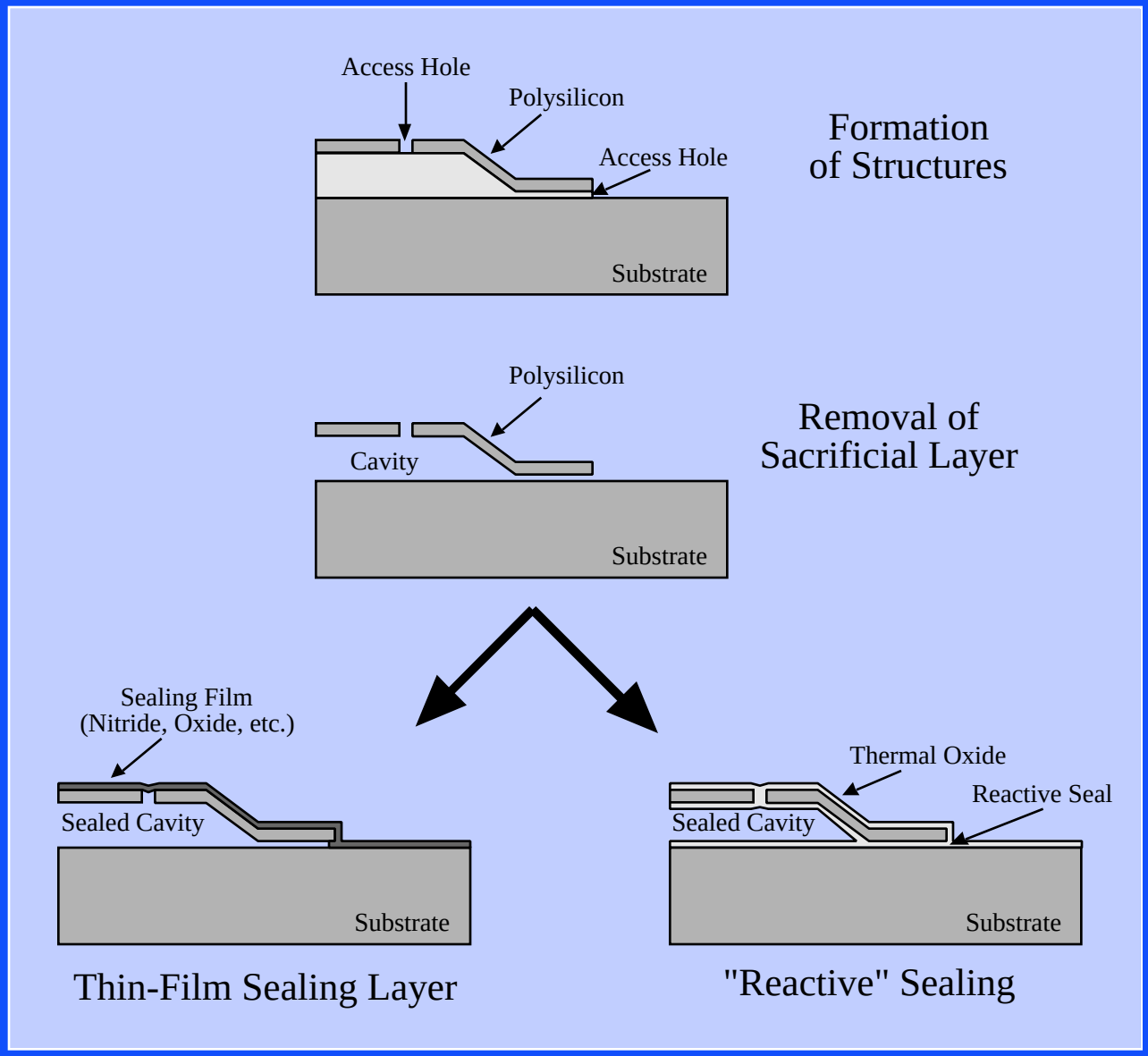


Courtesy of Chris Keller, U. C. Berkeley.



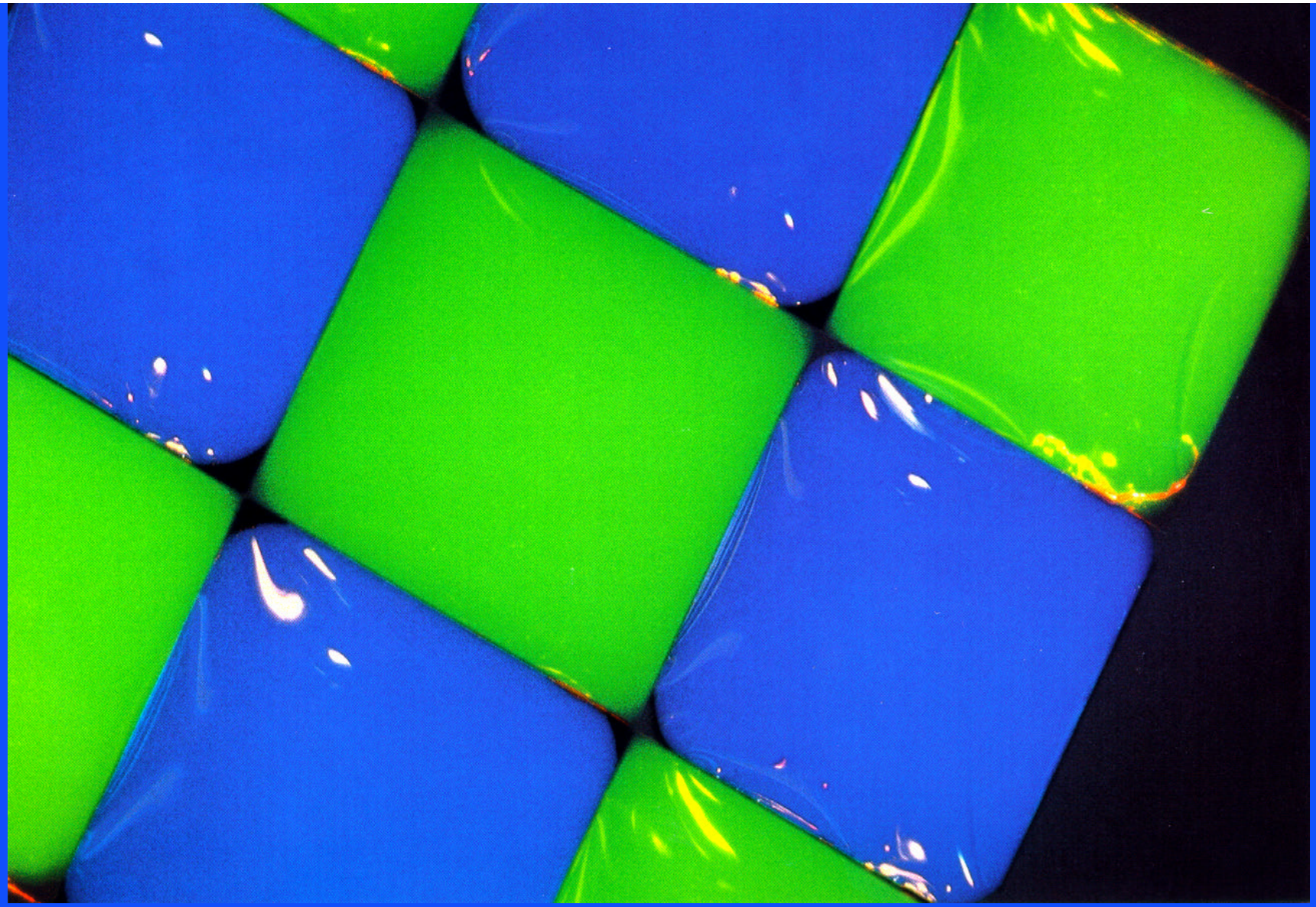
Courtesy of Chris Keller, U. C. Berkeley.

SEALED CAVITY FORMATION



SURFACE MODIFICATION

- **Chemical modifications of surfaces can play an important role in modifying wetting, friction, adhesion and other properties.**
- **Typically, so-called “self-assembled monolayers” (SAMs) are deposited on surfaces using silane or thiol chemistries.**
- **Octadecyltrichlorosilane (OTS) and (3,3,3-trifluororopyl) trichlorosilane (TFP) have been shown to significantly improve friction and wear with polysilicon mechanisms.**
- **SAMs can also be used to increase the selectivity of chemical sensors.**



Courtesy Prof. G. Whitesides. **Reference: Abbott, N. L, Folkers, J. P., and Whitesides, G. M., "Manipulation of the Wettability of Surfaces on the 0.1 - 1 Micrometer Scale Through Micromachining and Molecular Self-Assembly," Science, vol. 257, 1992, pp. 1380 - 1382.**

OTHER MICROMACHINING TECHNIQUES + ODDS & ENDS...

- **Electric Discharge Machining (EDM) can be used to serially micromachined structures.**
- **Stereolithography can be used to fabricate three-dimensional devices through stacking of sequential layers.**
- **If one can make a good enough mold, injection molding can resolve features in the few micron range.**
- **Waxes and even substances like Jello™can play important roles as temporary adhesives or protective layers.**

3D PATTERNING VIA TRANSFER PRINTING

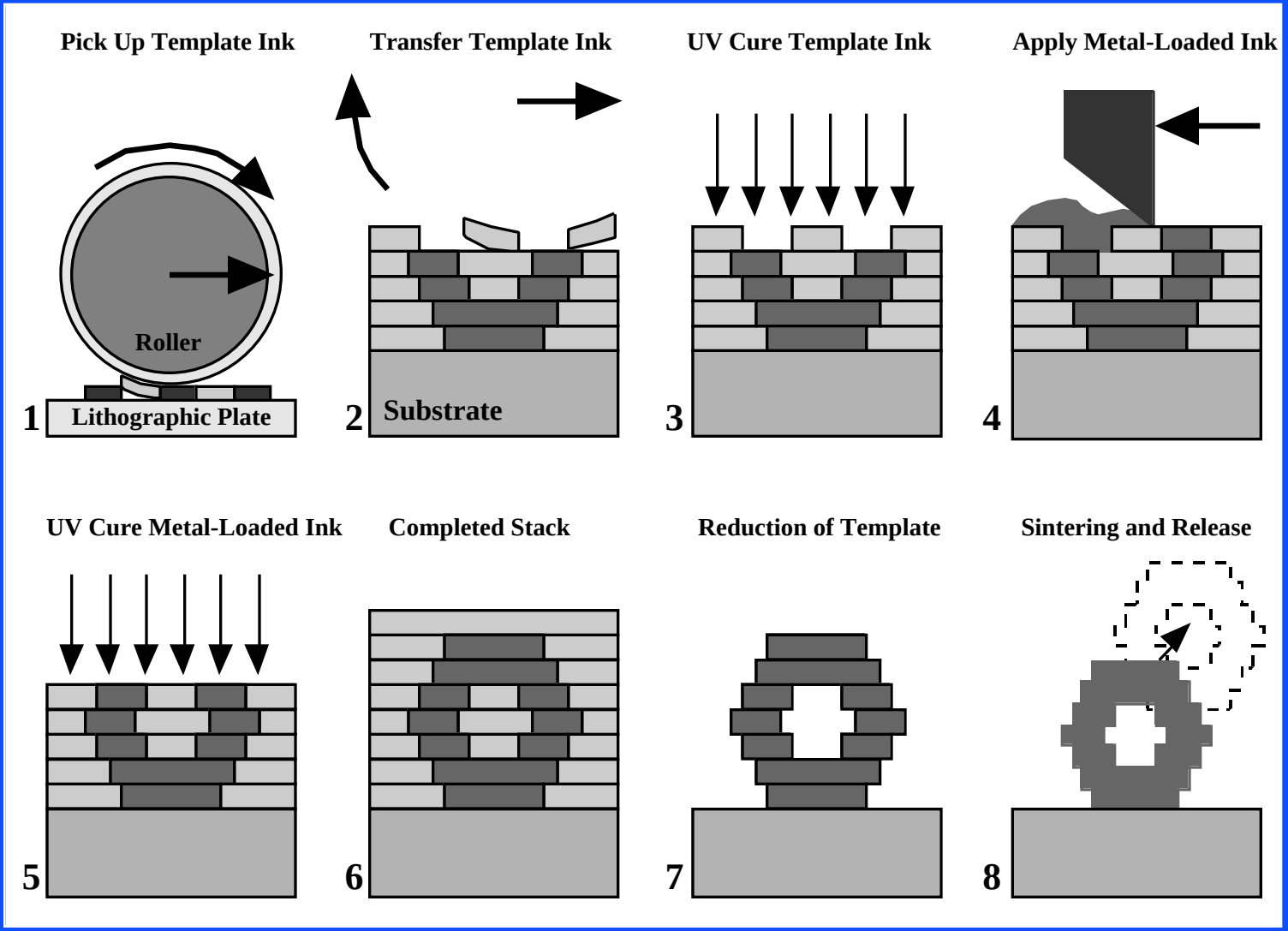
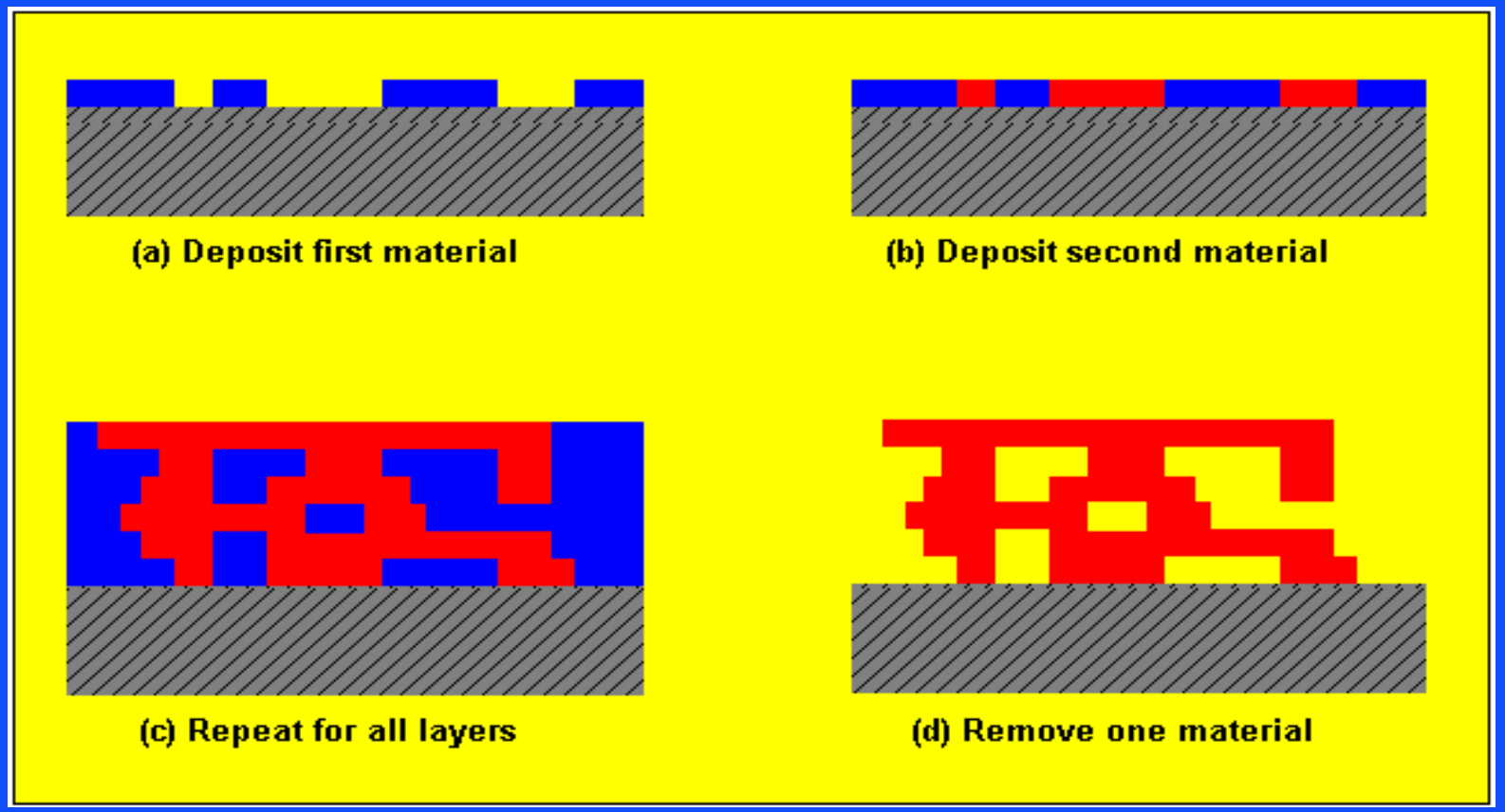
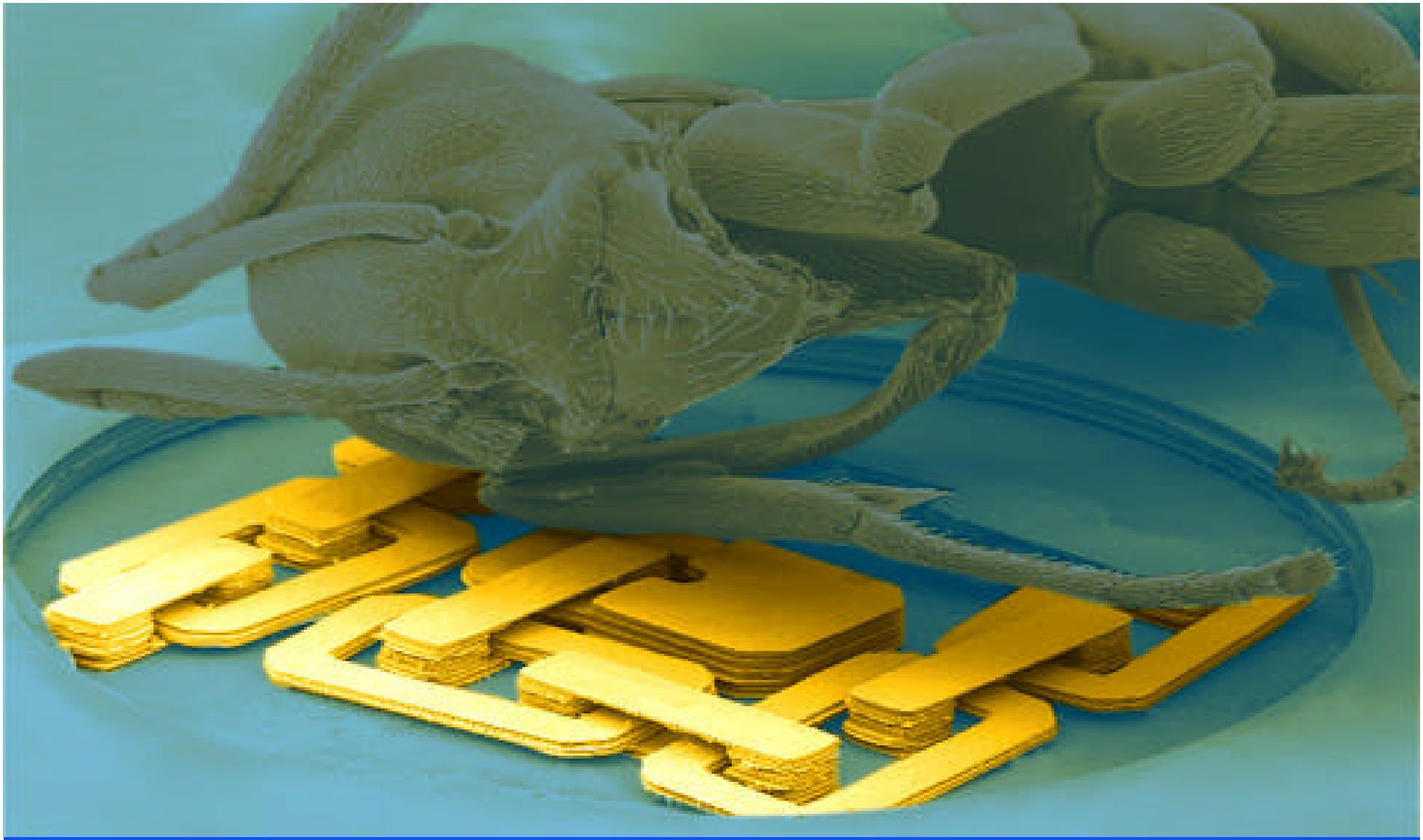


Illustration of the "spatial forming" process (after Taylor, et al., 1995).

EFAB COMMERCIAL PROCESS



http://www.isi.edu/efab/home.html



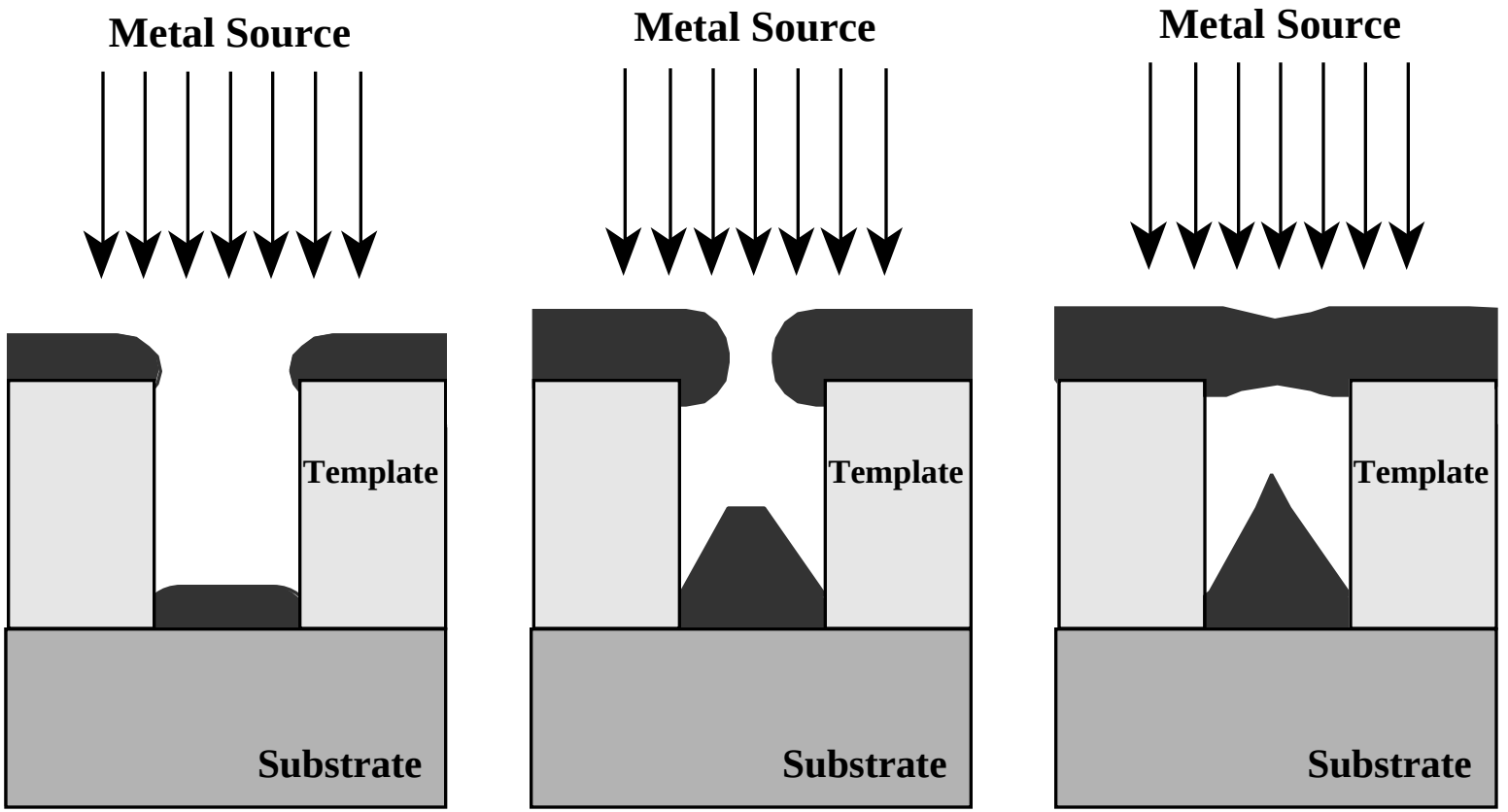
http://www.isi.edu/efab/home.html

http://www.isi.edu/efab/home.html

MICROMOLDING OF PLASTIC

Courtesy Prof. G. Whitesides. **Reference: Kim, E., Xia, Y., and Whitesides, G. M., "Polymer Microstructures Formed by Moulding in Capillaries," Nature, vol. 376, 1995, pp. 581 - 584.**

SPINDT TIP FORMATION



CHEMICAL-MECHANICAL POLISHING (CMP) FOR MICROSTRUCTURES

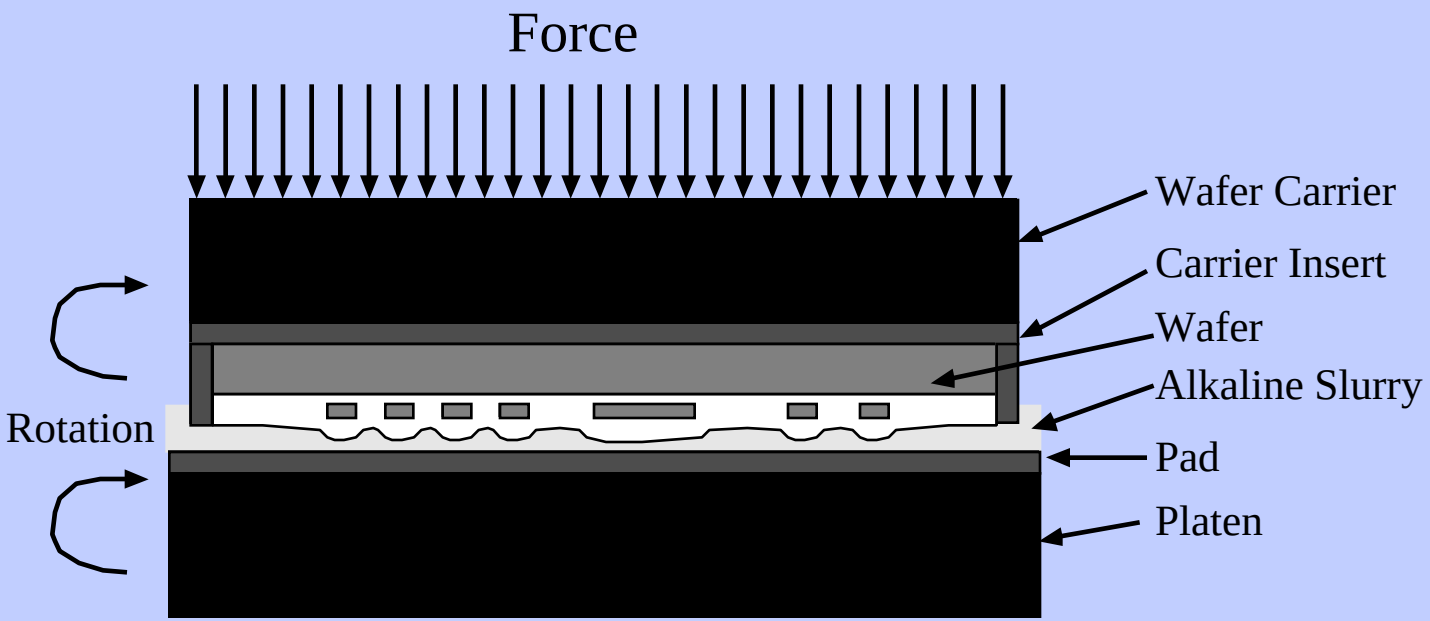
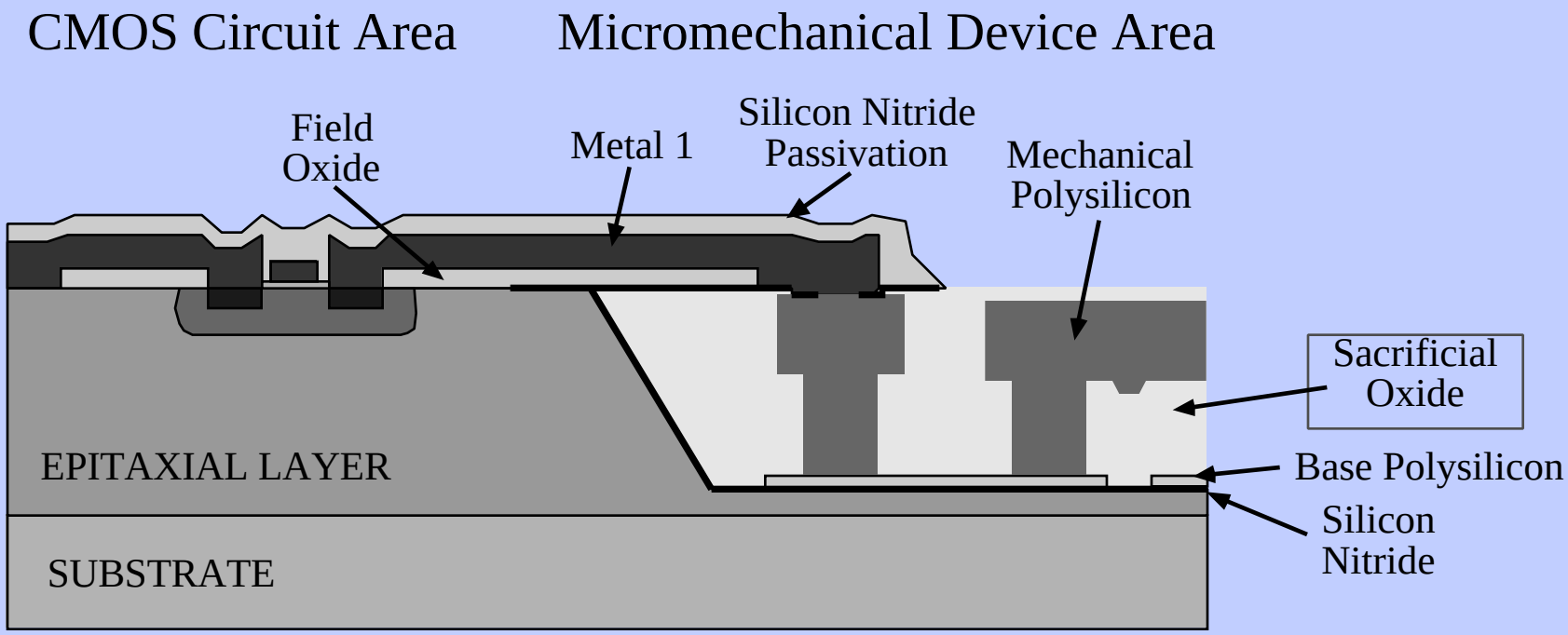
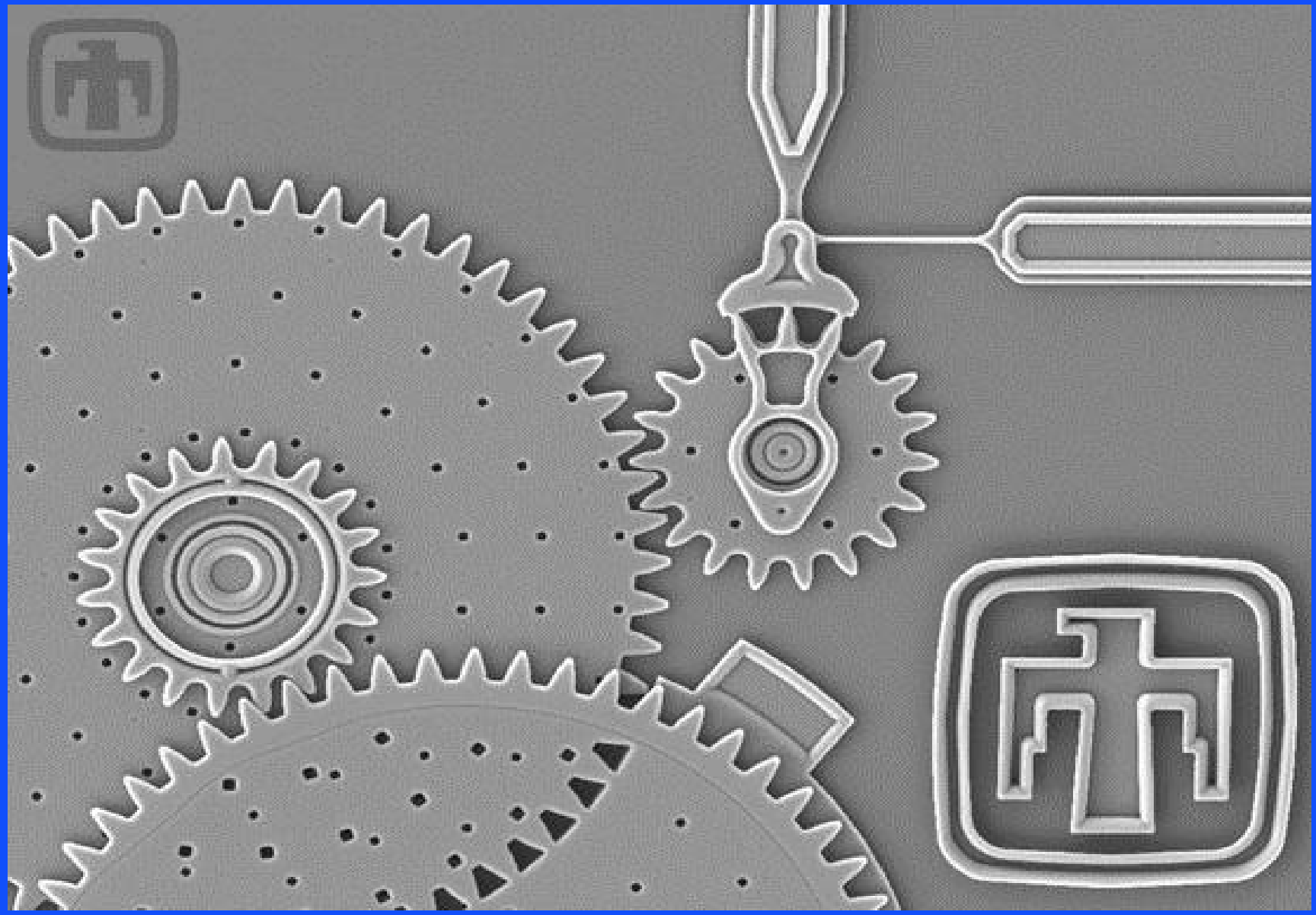


Illustration of the chemical-mechanical polishing (CMP) approach to planarizing integrated circuits (after Nasby, et al., (1996)).

CMP FOR "BURIED" MICROMECHANISMS

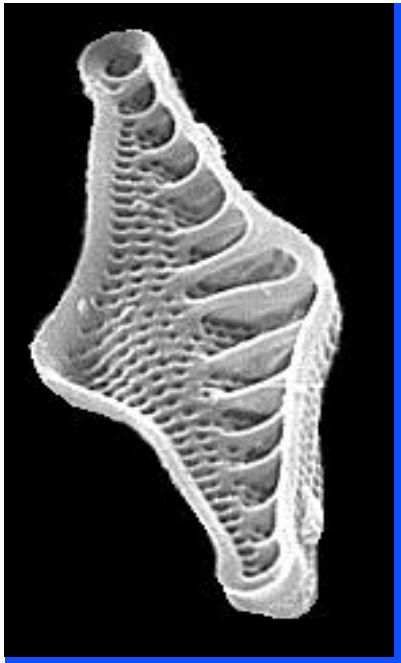


Simplified illustration of Nasby, et al.'s (1996) "buried" micromechanical polysilicon process with CMP planarization and CMOS post-fabrication (after Nasby, et al., (1996)).

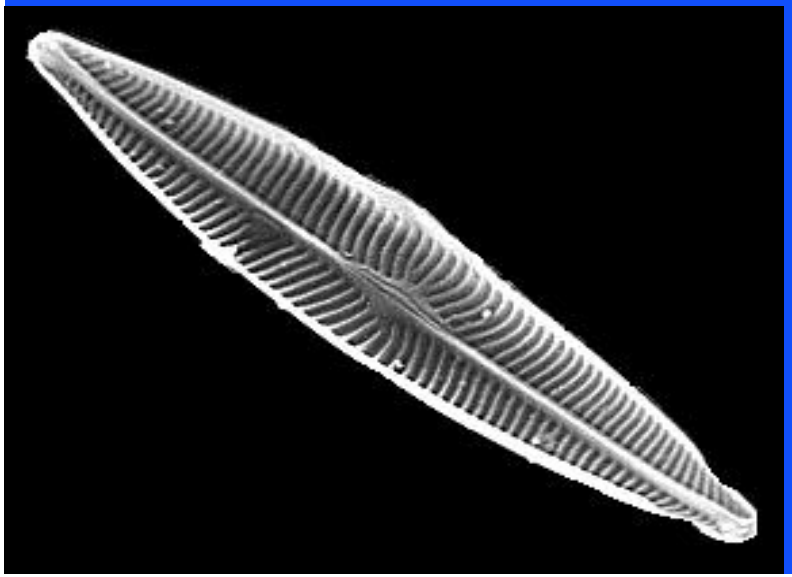


http://www.mdl.sandia.gov/Micromachine/images.html

MICROMACHINING IN NATURE



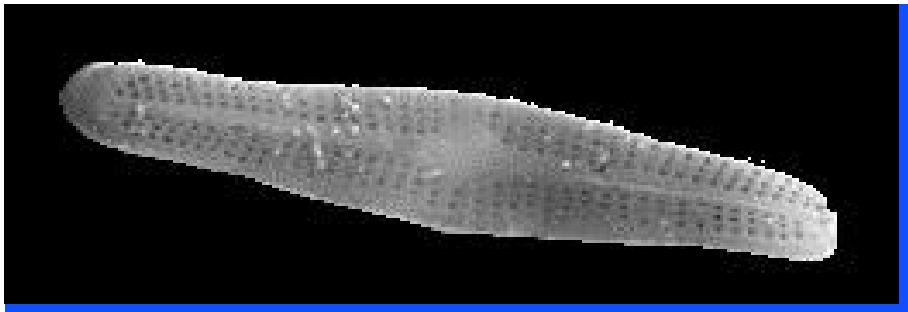
Key Source:
http://www.indiana.edu/~diatom/diatom.html

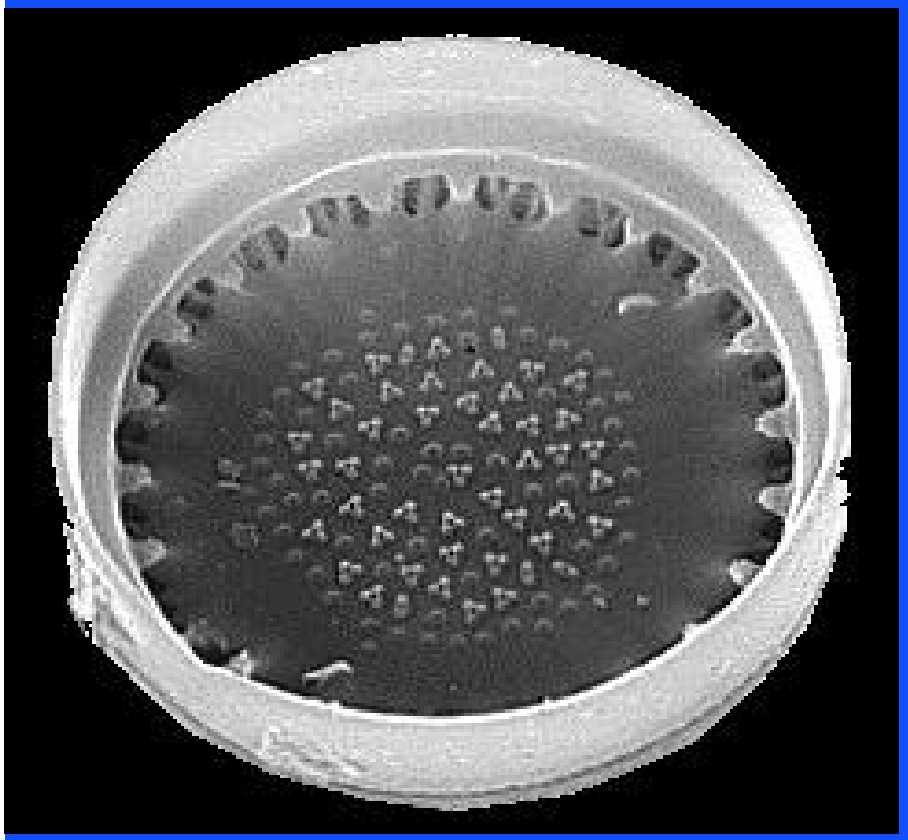


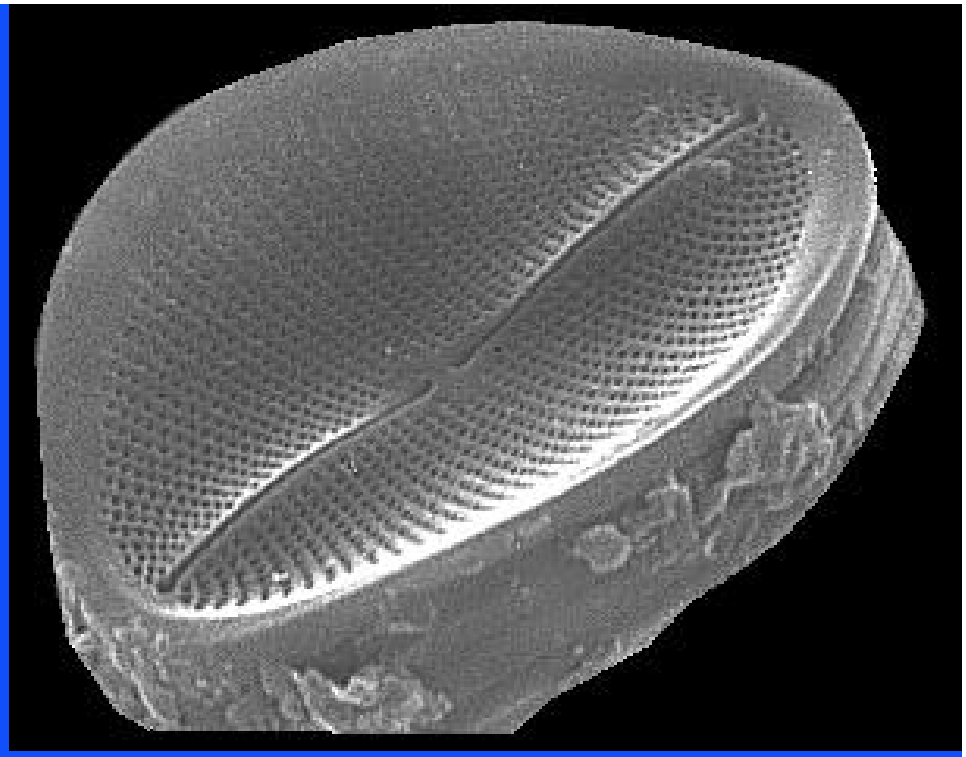
- **Diatoms are unicellular algae generally placed in the family Bacillariophyceae.**
- **The cell walls of these organisms are made of silica and are surprisingly complex in form.**
- **The cell walls are well preserved over time, allowing for historical surveys of algal life in aquatic systems.**

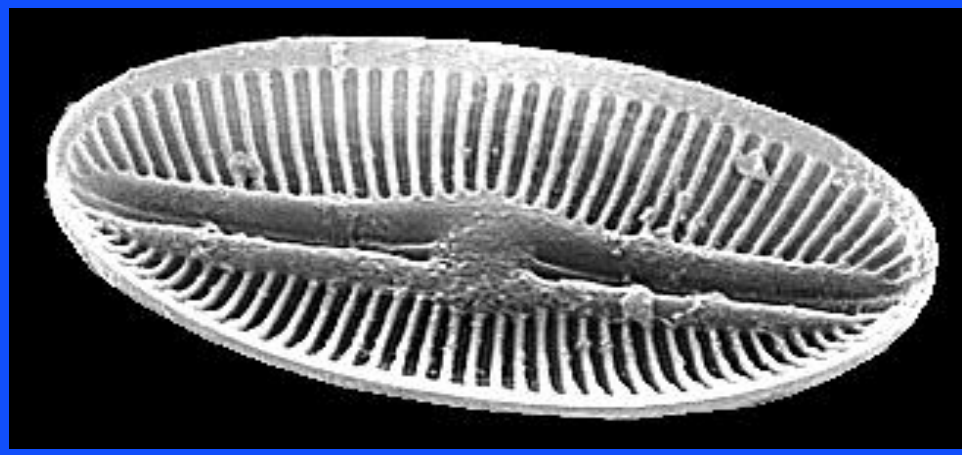
Source: Bowling Green University Center for Algal Microscopy and Image Digitization

http://www.bgsu.edu/departments/biology/algae/index.html









Source: Bowling Green University Center for Algal Microscopy and Image Digitization

http://www.bgsu.edu/departments/biology/algae/index.html